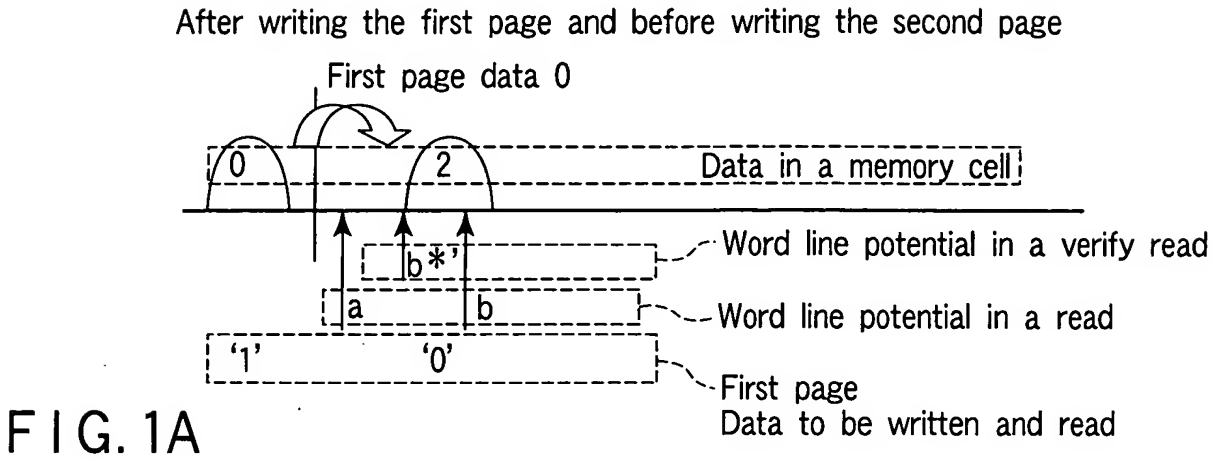

FIG. 1A

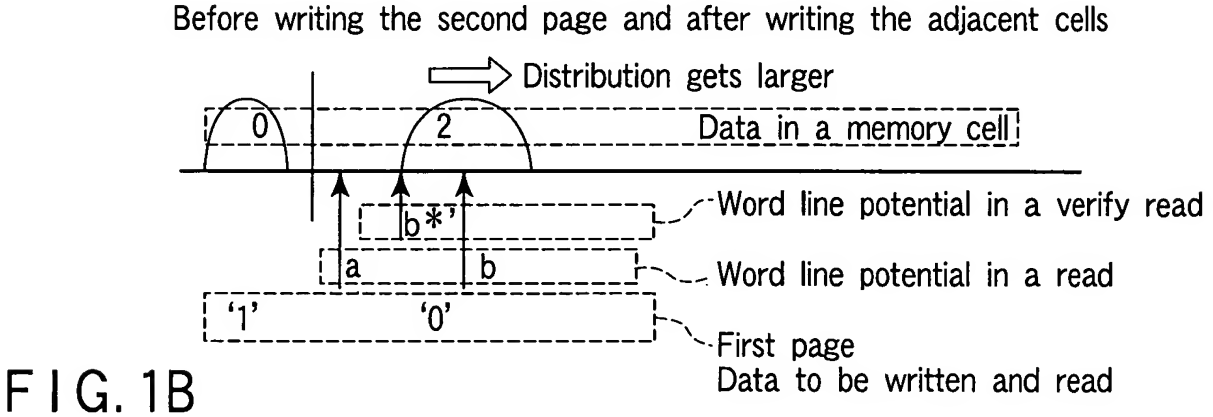

FIG. 1B

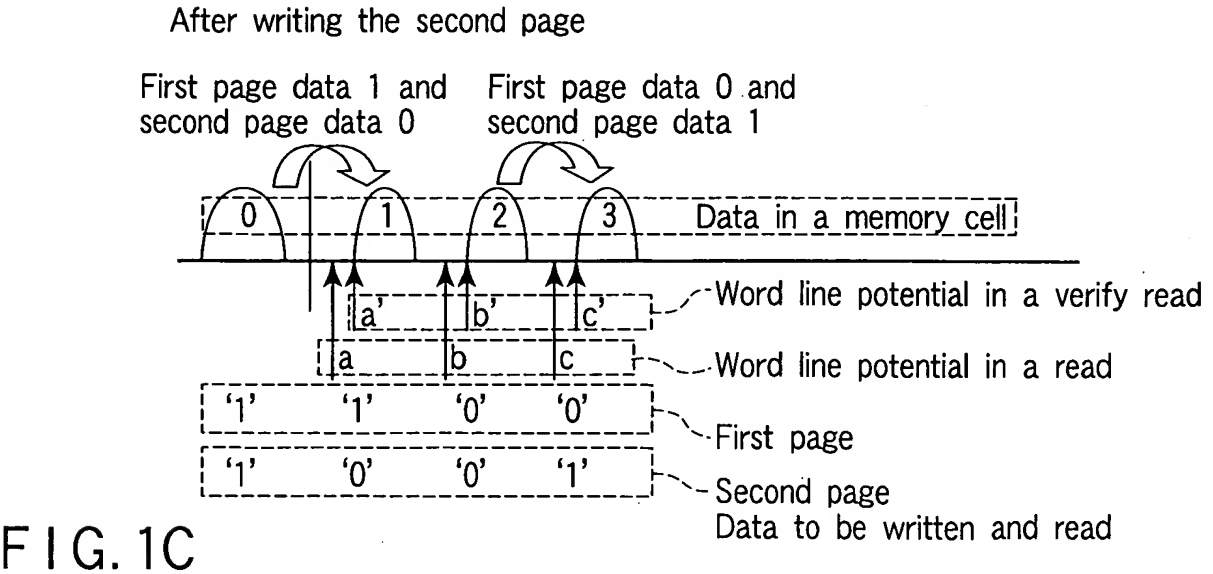

FIG. 1C

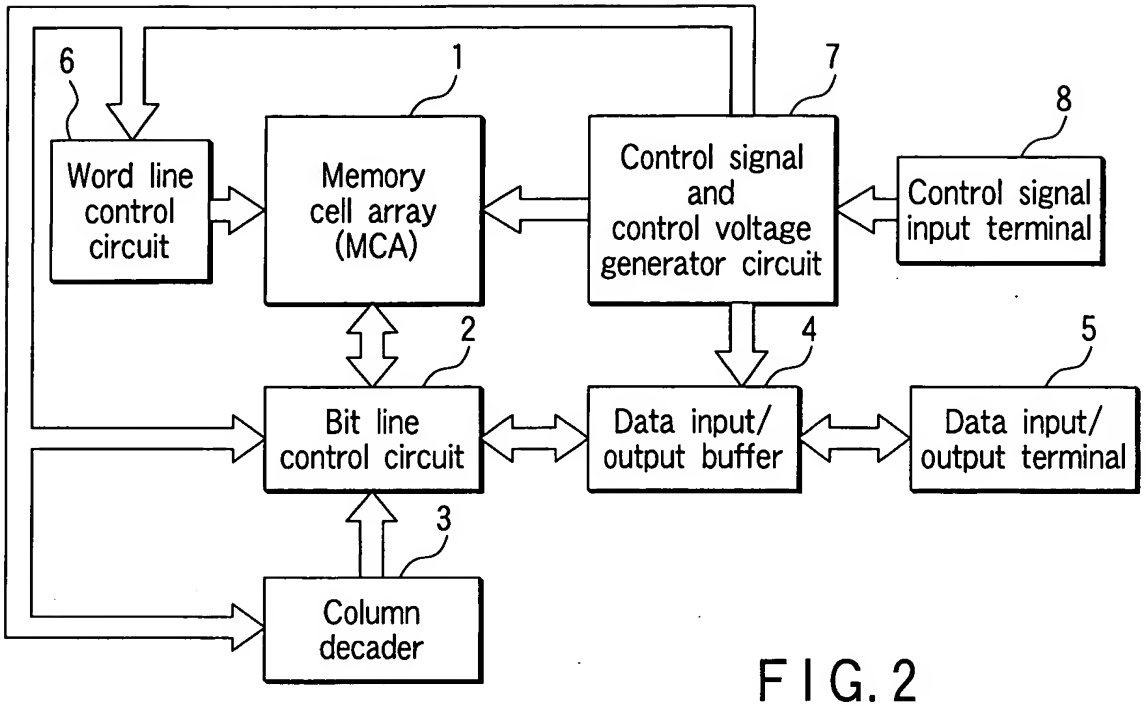

FIG. 2

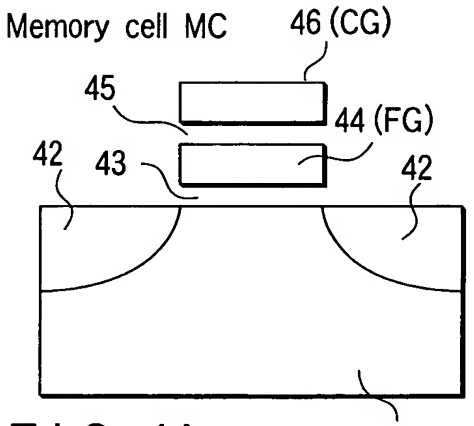

FIG. 4A

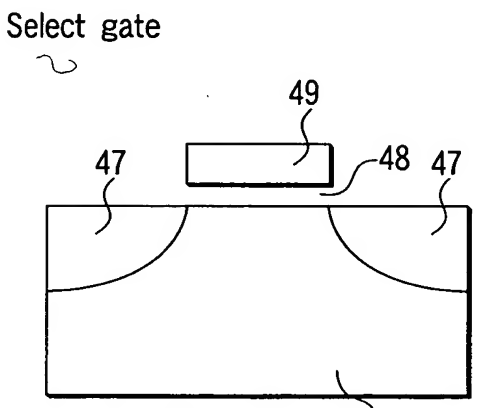

FIG. 4B

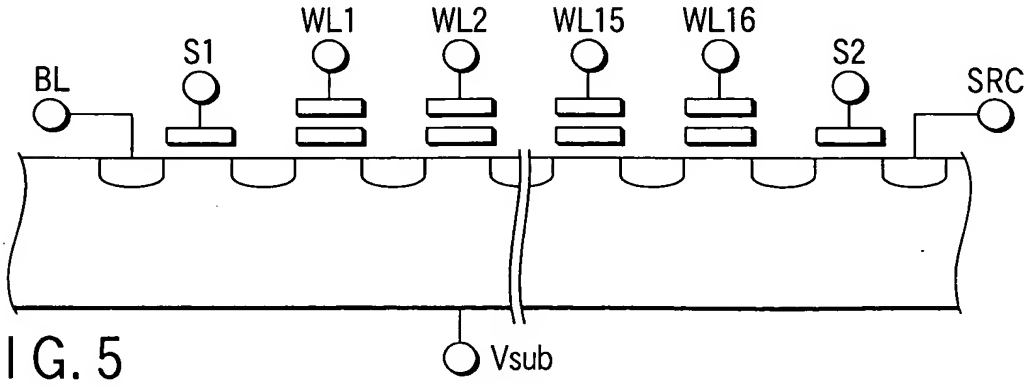

FIG. 5

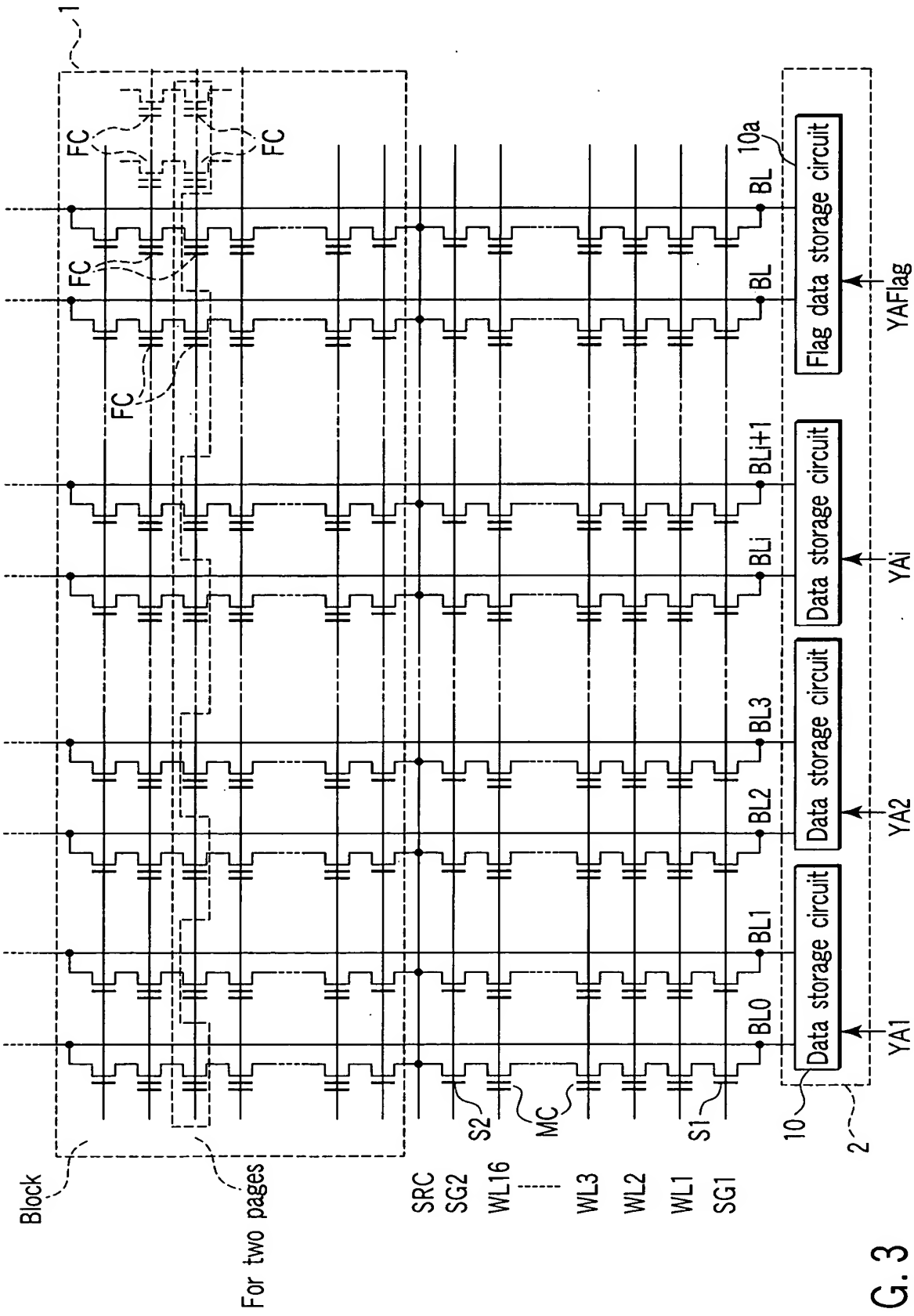
1
FC
FC
FC
FC
BL
BL
10a
BLi+1
BLi
BL3
BL2
BL1
BL0
Flag data storage circuit
Data storage circuit
Data storage circuit
Data storage circuit
Data storage circuit
YAFlag
YAi
YA2
YA1
10
2
S2
MC
S1
Block
For two pages
SRC
SG2
WL16
WL3
WL2
WL1
SG1

FIG. 3

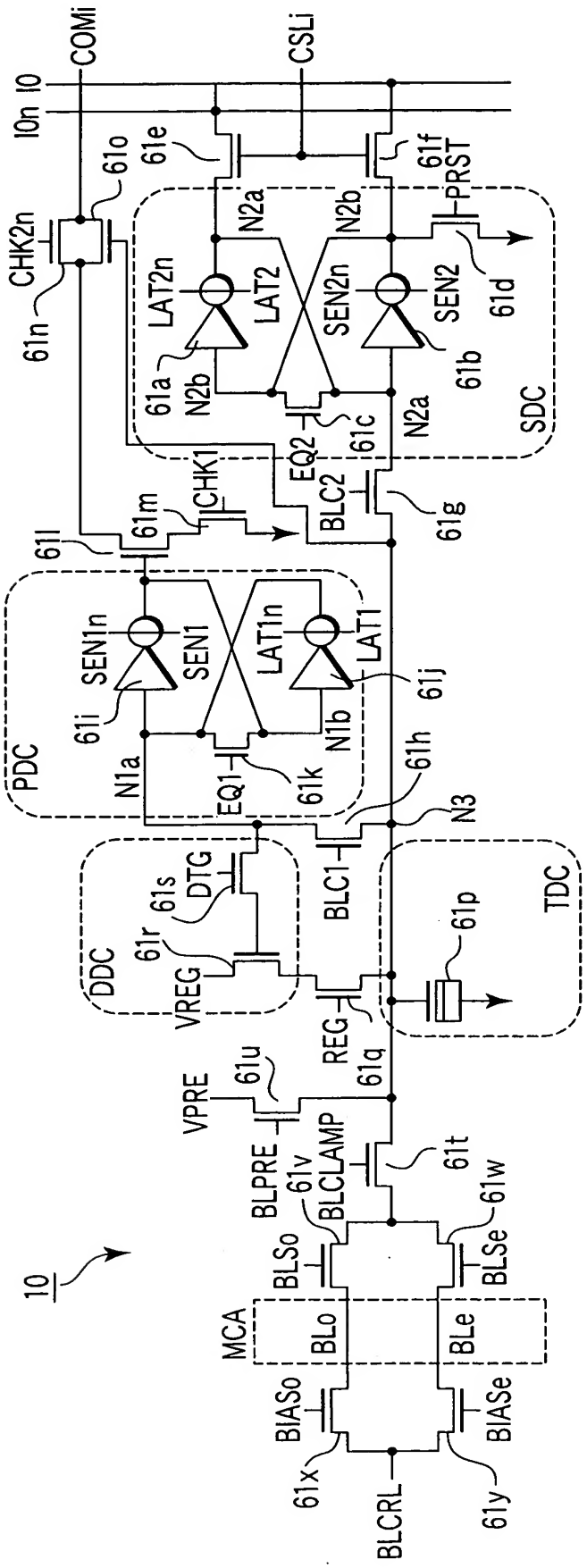
COMi
CSLi
IO
IOn
61o
61e
61f
PRST
CHK2n
61n
N2a
N2b
LAT2n
LAT2
SEN2n
SEN2
61d
61a
61b
SDC
EQ2
61c
CHK1
BLC2
61g
61m
61l
SEN1n
SEN1
LAT1n
LAT1
61j
61i
PDC
N1a
N1b
EQ1
61k
61h
N3
BLC1
61s
DTG
61r
DDC
VREG
61p
TDC
REG
61q
VPRE
61u
BLPRE
61v
BLCLAMP
61t
61w
BLSo
BLSe
MCA
BLo
BLe
BIASo
BIASe
61x
61y
BLCRL
10

FIG. 6

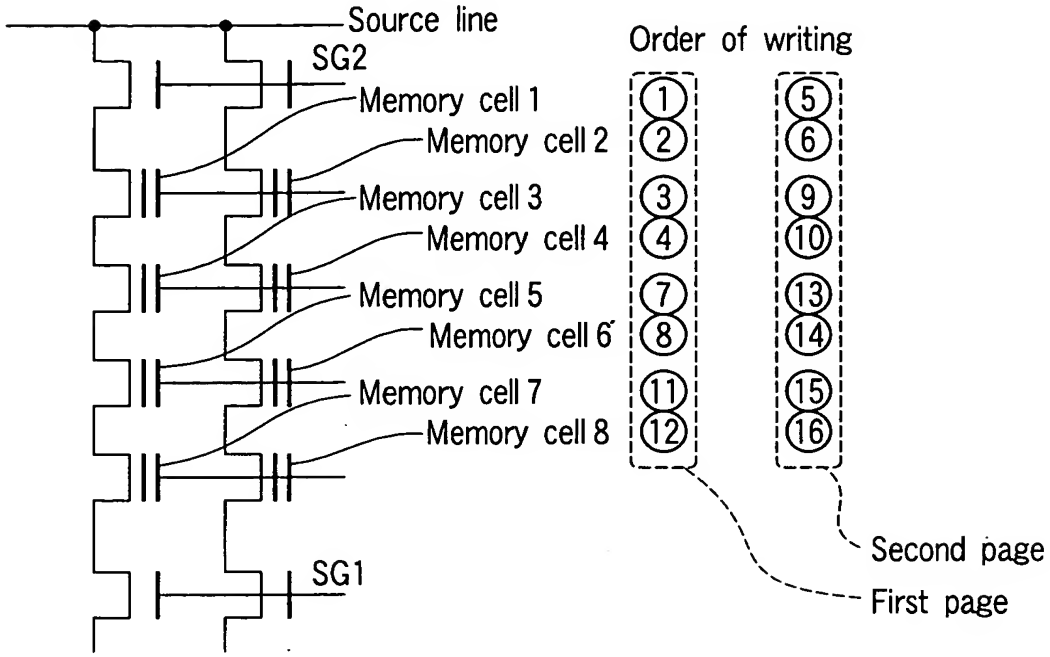
Source line
SG2
Memory cell 1
Memory cell 2
Memory cell 3
Memory cell 4
Memory cell 5
Memory cell 6
Memory cell 7
Memory cell 8
SG1
Order of writing
1
2
3
4
7
8
11
12
5
6
9
10
13
14
15
16
Second page
First page

FIG. 7

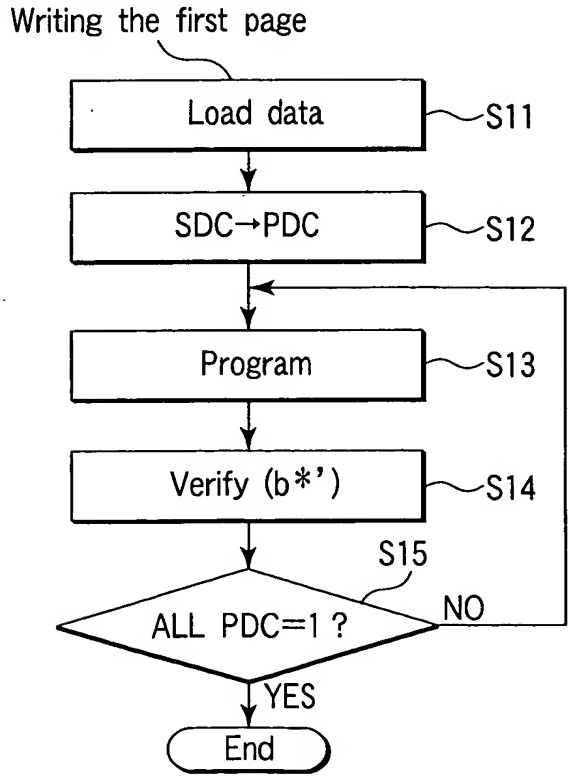
Writing the first page
Load data
S11
SDC→PDC
S12
Program
S13
Verify (b*')
S14
S15
ALL PDC=1 ?
NO
YES
End

FIG. 8

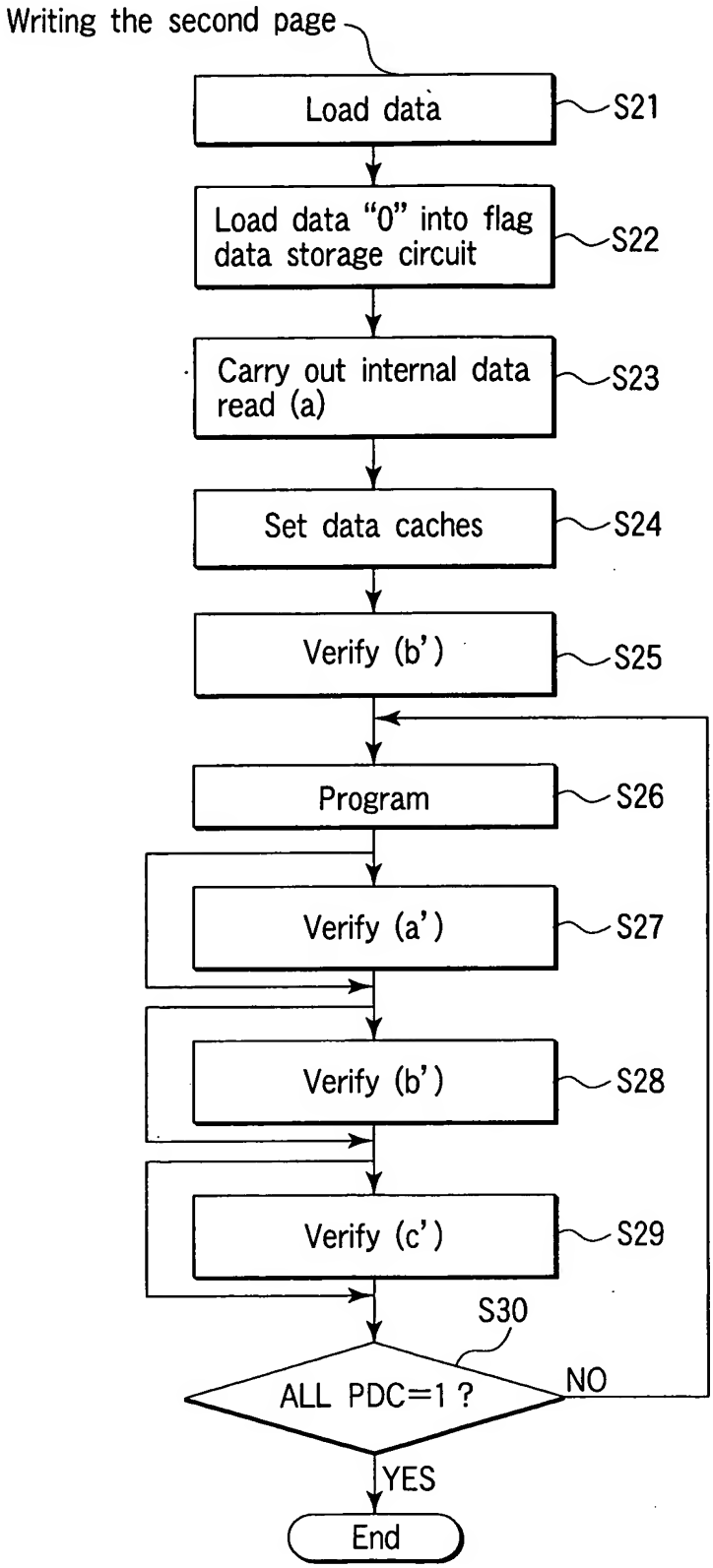
Writing the second page
Load data
S21
Load data "0" into flag data storage circuit
S22
Carry out internal data read (a)
S23
Set data caches
S24
Verify (b')
S25
Program
S26
Verify (a')
S27
Verify (b')
S28
Verify (c')
S29
S30
ALL PDC=1 ?
NO
YES
End

FIG. 9

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 10A

After setting data caches

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 10B

Data cache setting procedure

SDC				DDC				PDC				TDC				
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	Data in memory cell after writing
1	0	0	1					0	0	1	1					After internal data read
1	0	0	1	0	0	1	1	0	0	1	1					Copy data in PDC into DDC
1	0	0	1	0	0	1	1	1	0	0	1					Copy data in SDC into PDC
1	0	0	1	0	0	1	1	1	0	0	0	1	1	1	1	TDC=H
1	0	0	1	0	0	1	1	1	0	0	1	1	1	0	0	VREG=L, REG=H
1	1	0	0	0	0	1	1	1	0	0	1	1	1	0	0	Copy data in TDC into SDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1	Copy data in PDC into TDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	0	VREG=L, REG=H
1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	0	Copy data in PDC into DDC
1	1	0	0	1	0	0	1	1	0	0	0	1	0	0	0	Copy data in TDC into PDC

FIG. 11

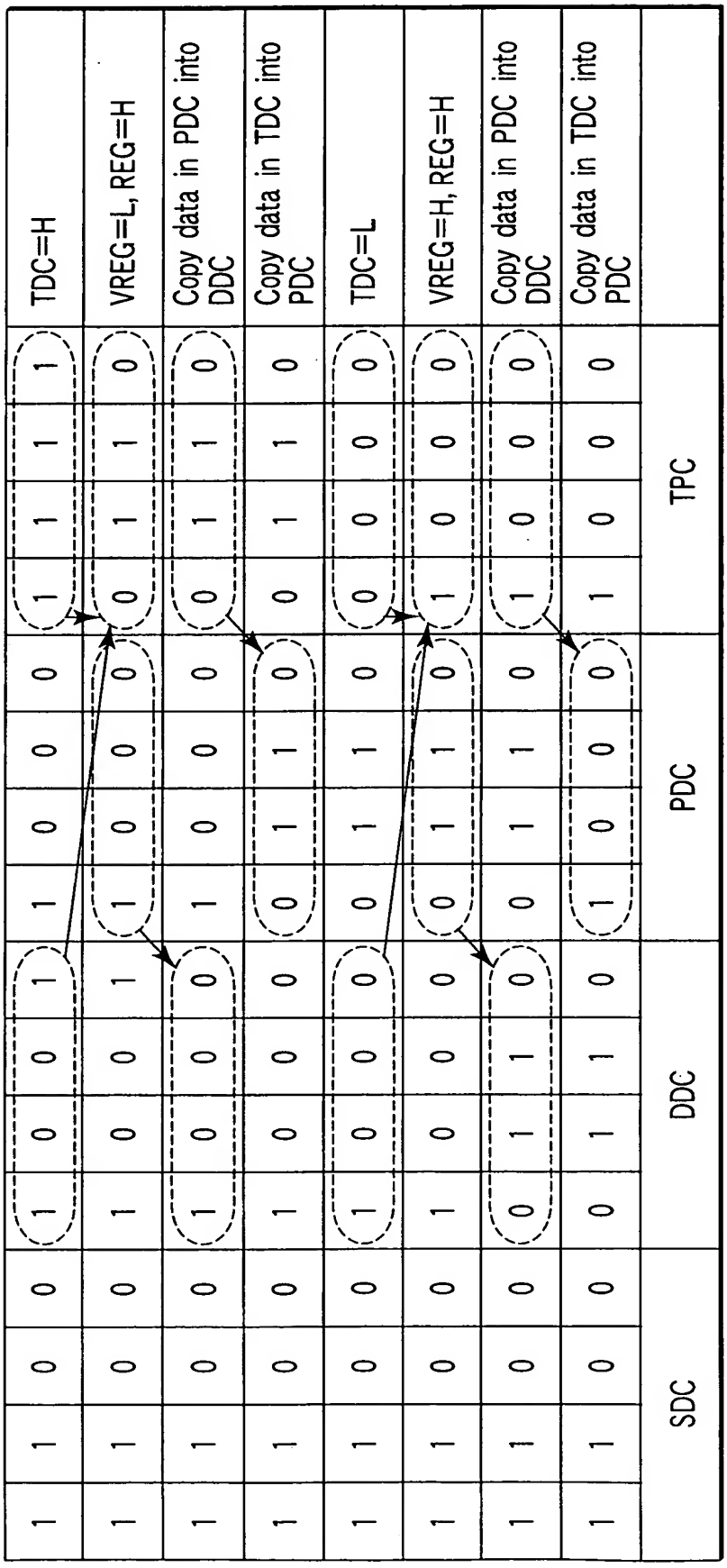
TDC=H
VREG=L, REG=H
Copy data in PDC into DDC
Copy data in TDC into PDC
TDC=L
VREG=H, REG=H
Copy data in PDC into DDC
Copy data in TDC into PDC
SDC
DDC
PDC
TPC

FIG. 12

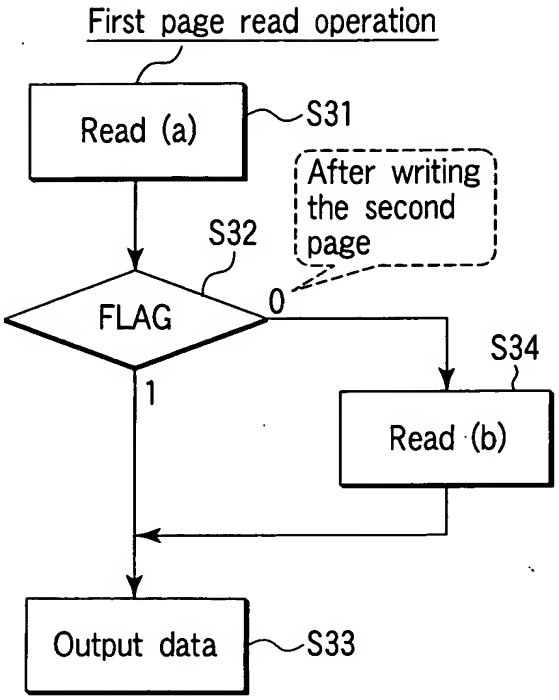

FIG. 13

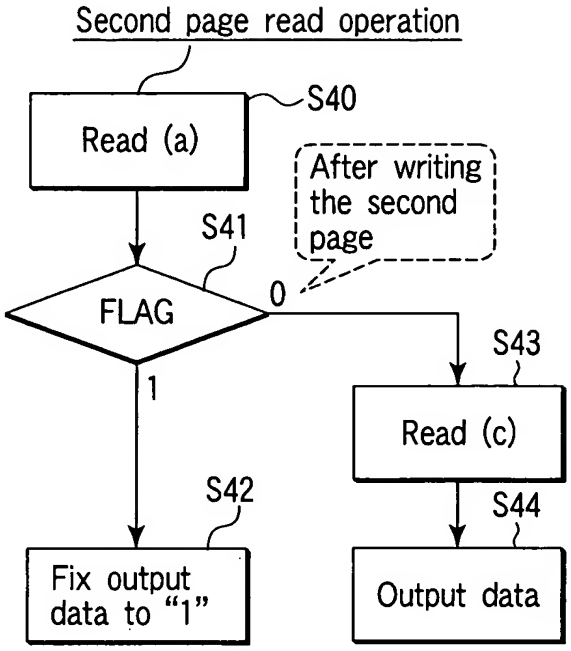

FIG. 15

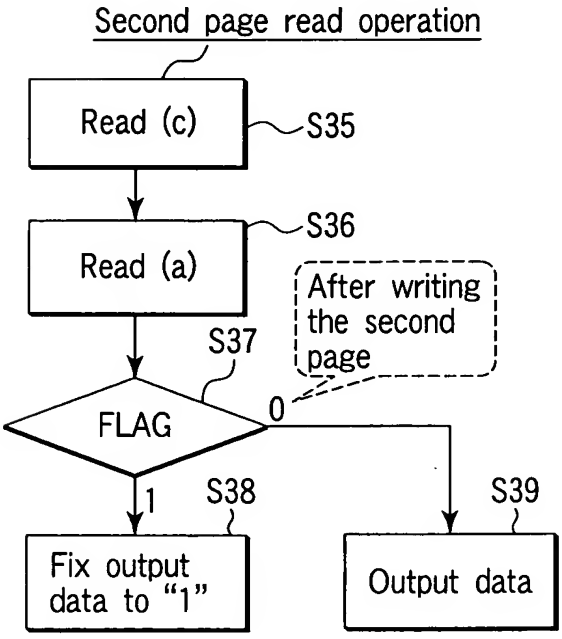

FIG. 14

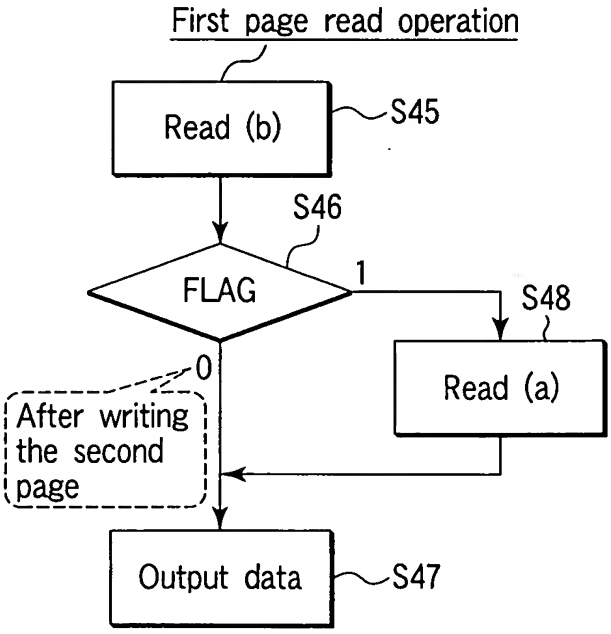

FIG. 16

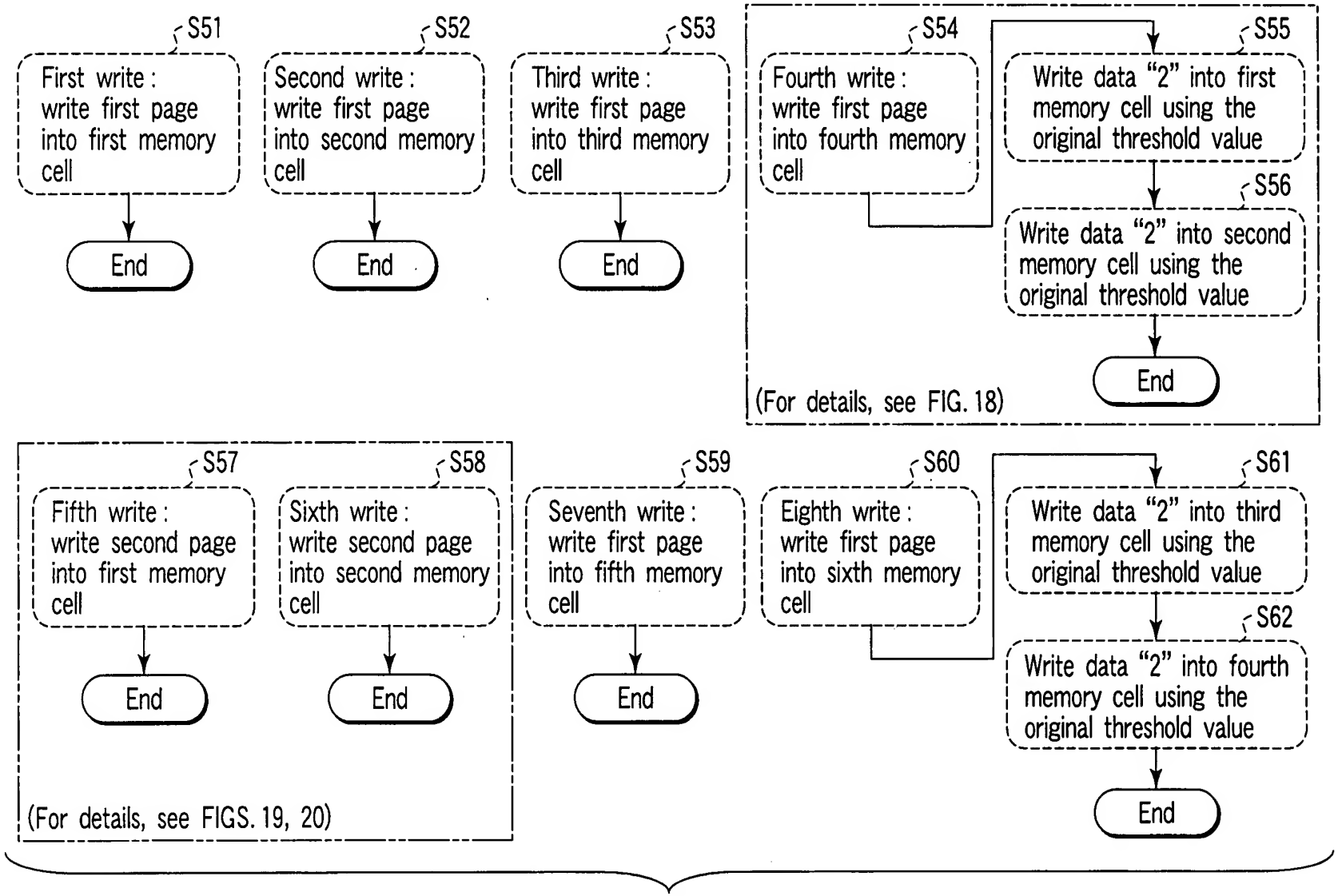
S51
First write : write first page into first memory cell
End
S52
Second write : write first page into second memory cell
End
S53
Third write : write first page into third memory cell
End
S54
Fourth write : write first page into fourth memory cell
S55
Write data "2" into first memory cell using the original threshold value
S56
Write data "2" into second memory cell using the original threshold value
End
(For details, see FIG. 18)
S57
Fifth write : write second page into first memory cell
End
S58
Sixth write : write second page into second memory cell
End
(For details, see FIGS. 19, 20)
S59
Seventh write : write first page into fifth memory cell
End
S60
Eighth write : write first page into sixth memory cell
S61
Write data "2" into third memory cell using the original threshold value
S62
Write data "2" into fourth memory cell using the original threshold value
End

FIG. 17

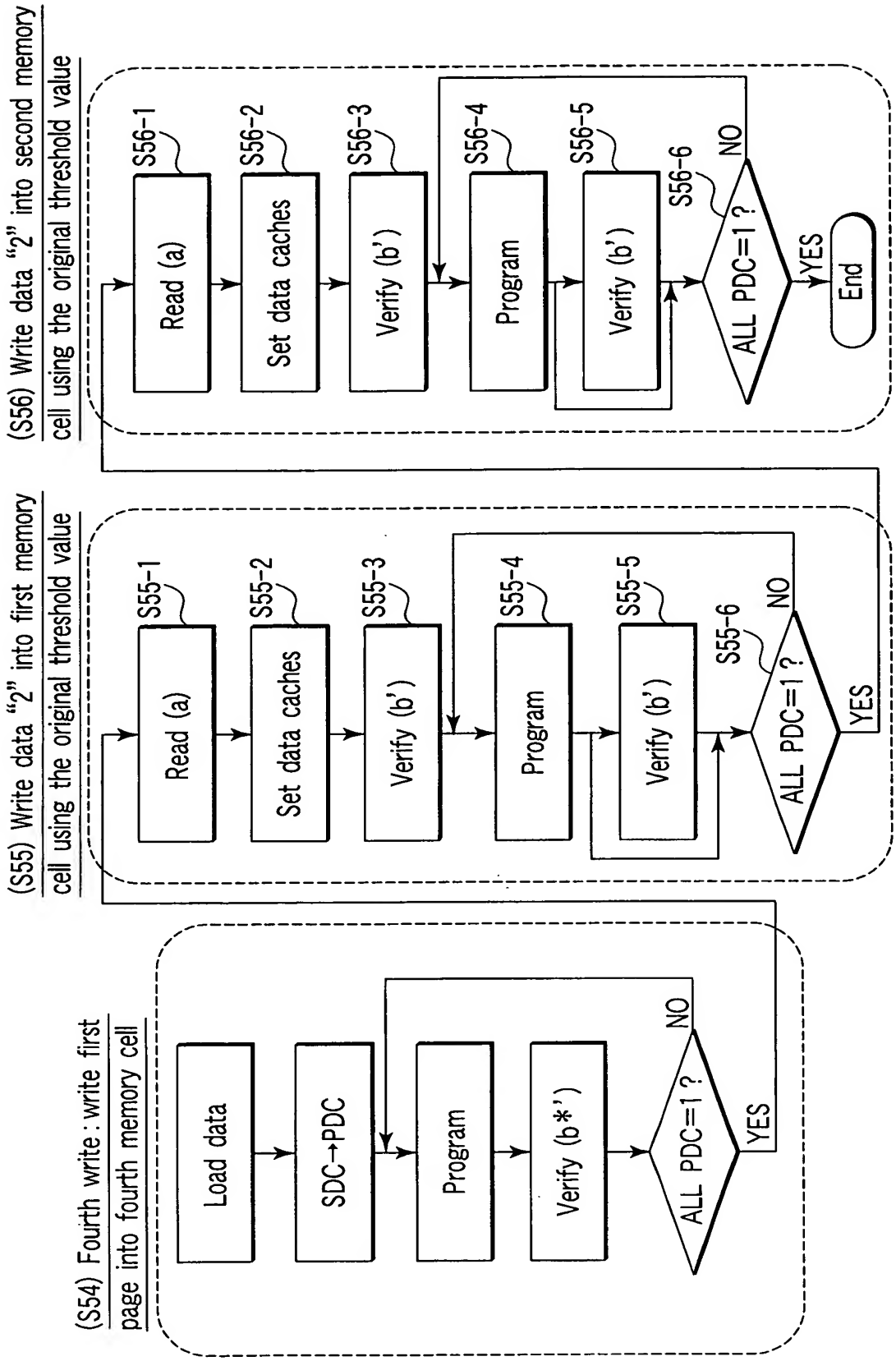
(S54) Fourth write : write first page into fourth memory cell
Load data
SDC→PDC
Program
Verify (b*')
ALL PDC=1 ?
NO
YES
(S55) Write data "2" into first memory cell using the original threshold value
S55-1
Read (a)
S55-2
Set data caches
S55-3
Verify (b')
S55-4
Program
S55-5
Verify (b')
S55-6
ALL PDC=1 ?
NO
YES
(S56) Write data "2" into second memory cell using the original threshold value
S56-1
Read (a)
S56-2
Set data caches
S56-3
Verify (b')
S56-4
Program
S56-5
Verify (b')
S56-6
ALL PDC=1 ?
NO
YES
End

FIG. 18

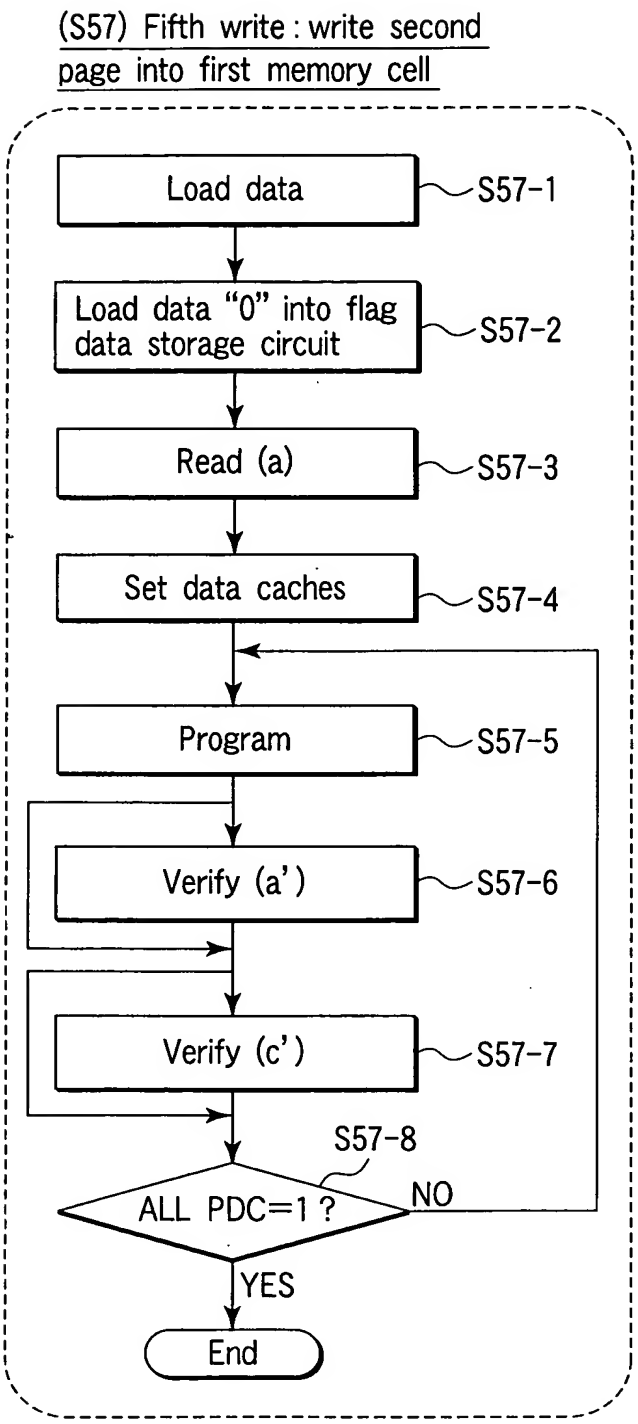
(S57) Fifth write : write second page into first memory cell
Load data
S57-1
Load data "0" into flag data storage circuit
S57-2
Read (a)
S57-3
Set data caches
S57-4
Program
S57-5
Verify (a')
S57-6
Verify (c')
S57-7
S57-8
ALL PDC=1 ?
NO
YES
End

FIG. 19

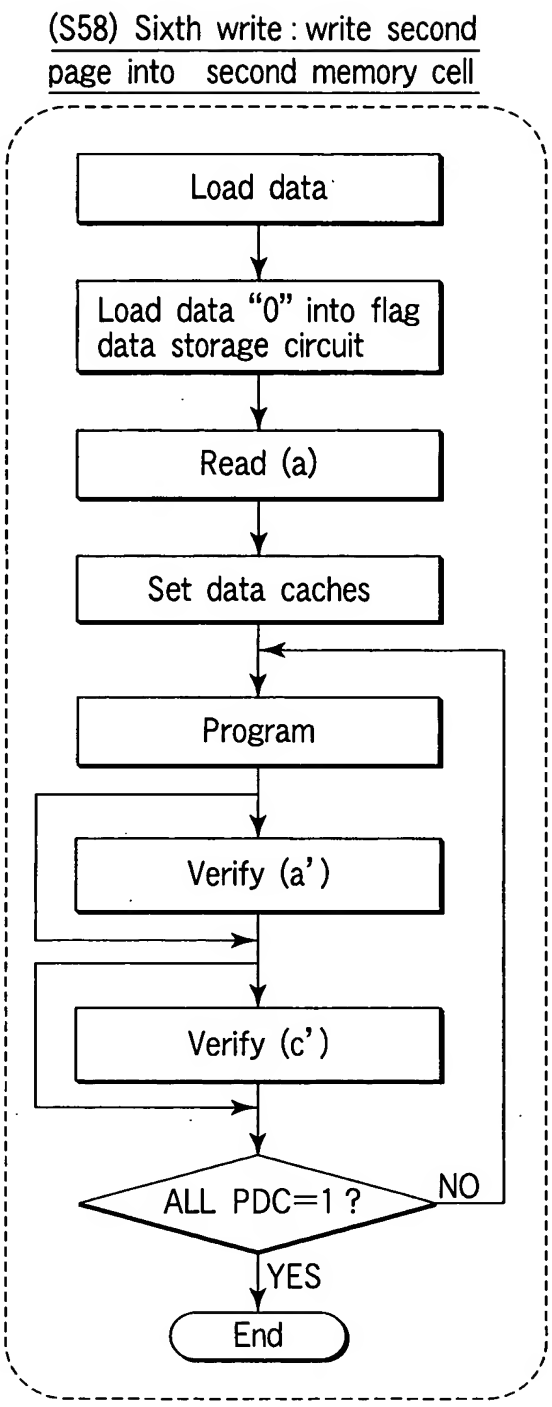
(S58) Sixth write : write second page into second memory cell
Load data
Load data "0" into flag data storage circuit
Read (a)
Set data caches
Program
Verify (a')
Verify (c')
ALL PDC=1 ?
NO
YES
End

FIG. 20

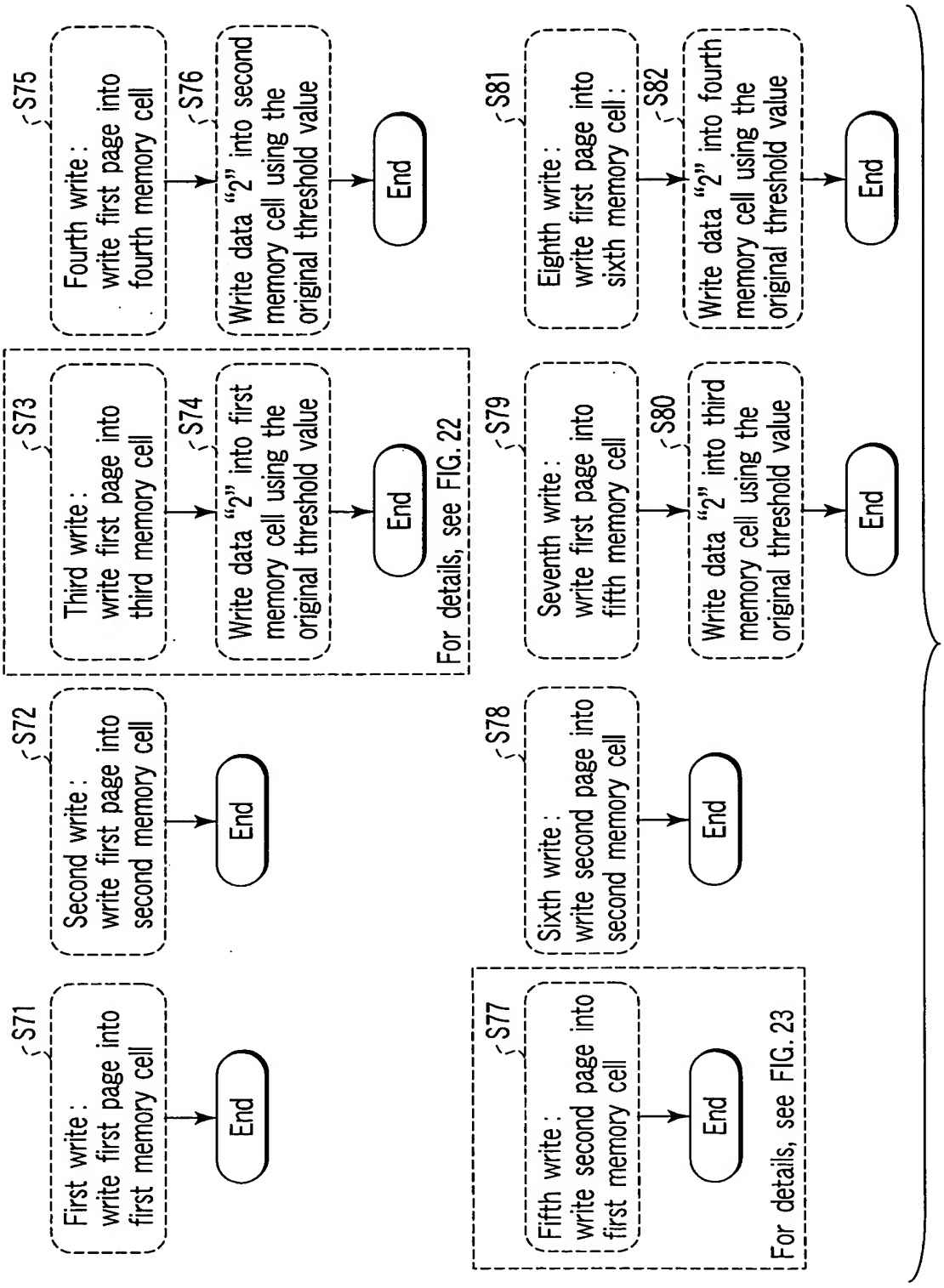
S71
First write : write first page into first memory cell
End
S72
Second write : write first page into second memory cell
End
S73
Third write : write first page into third memory cell
S74
Write data "2" into first memory cell using the original threshold value
End
For details, see FIG. 22
S75
Fourth write : write first page into fourth memory cell
S76
Write data "2" into second memory cell using the original threshold value
End
S77
Fifth write : write second page into first memory cell
End
For details, see FIG. 23
S78
Sixth write : write second page into second memory cell
End
S79
Seventh write : write first page into fifth memory cell
S80
Write data "2" into third memory cell using the original threshold value
End
S81
Eighth write : write first page into sixth memory cell :
S82
Write data "2" into fourth memory cell using the original threshold value
End

FIG. 21

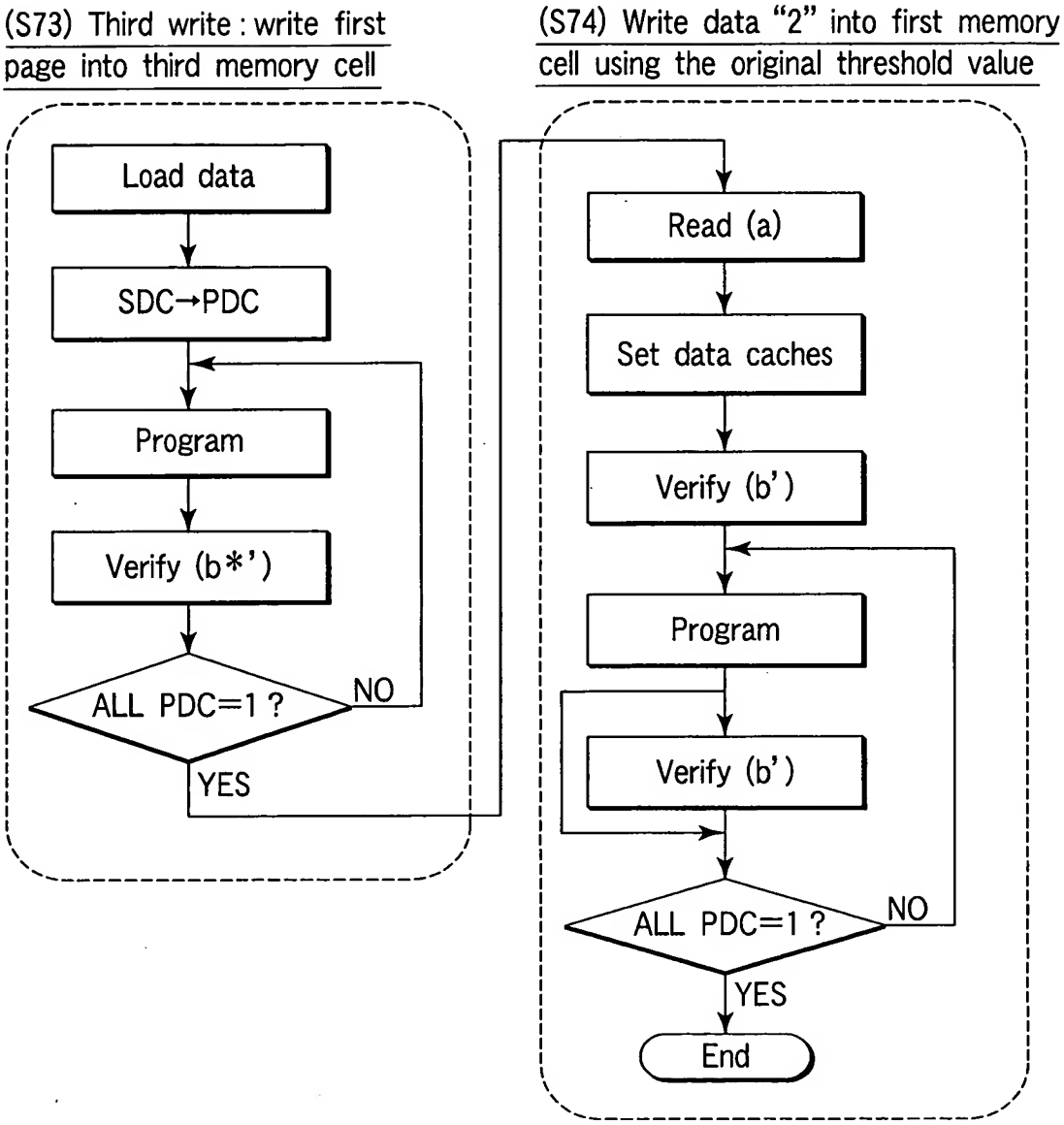
(S73) Third write : write first page into third memory cell
Load data
SDC→PDC
Program
Verify (b*')
ALL PDC=1 ?
NO
YES
(S74) Write data "2" into first memory cell using the original threshold value
Read (a)
Set data caches
Verify (b')
Program
Verify (b')
ALL PDC=1 ?
NO
YES
End

FIG. 22

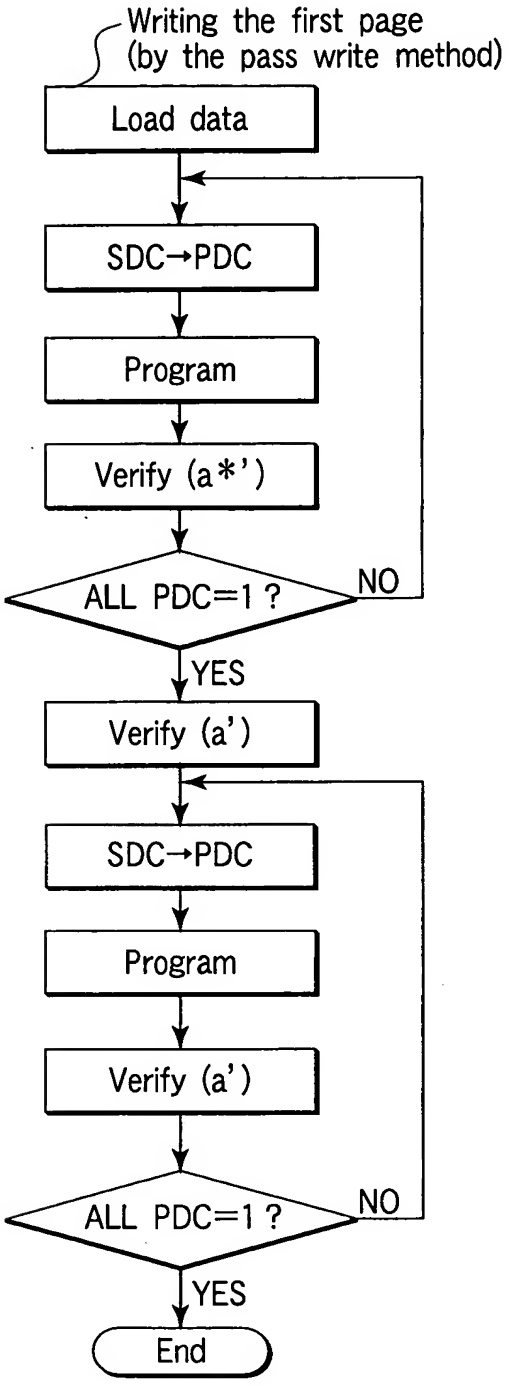

FIG. 23A

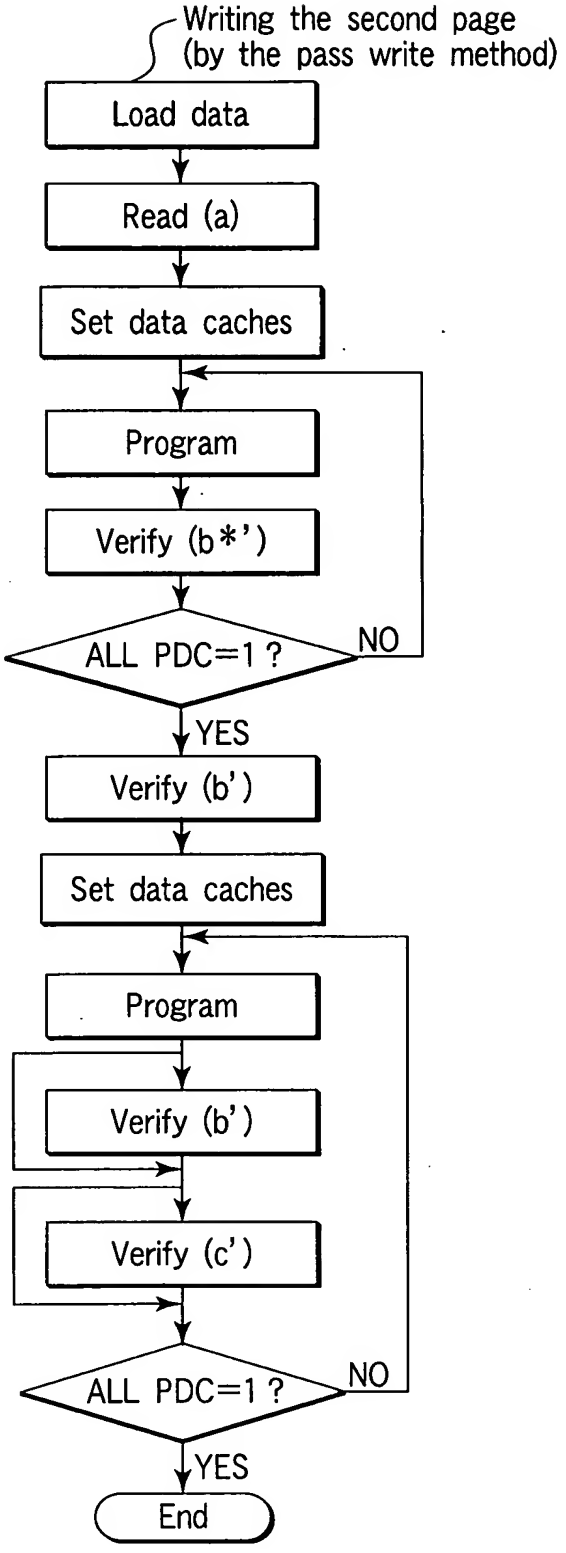

FIG. 23B

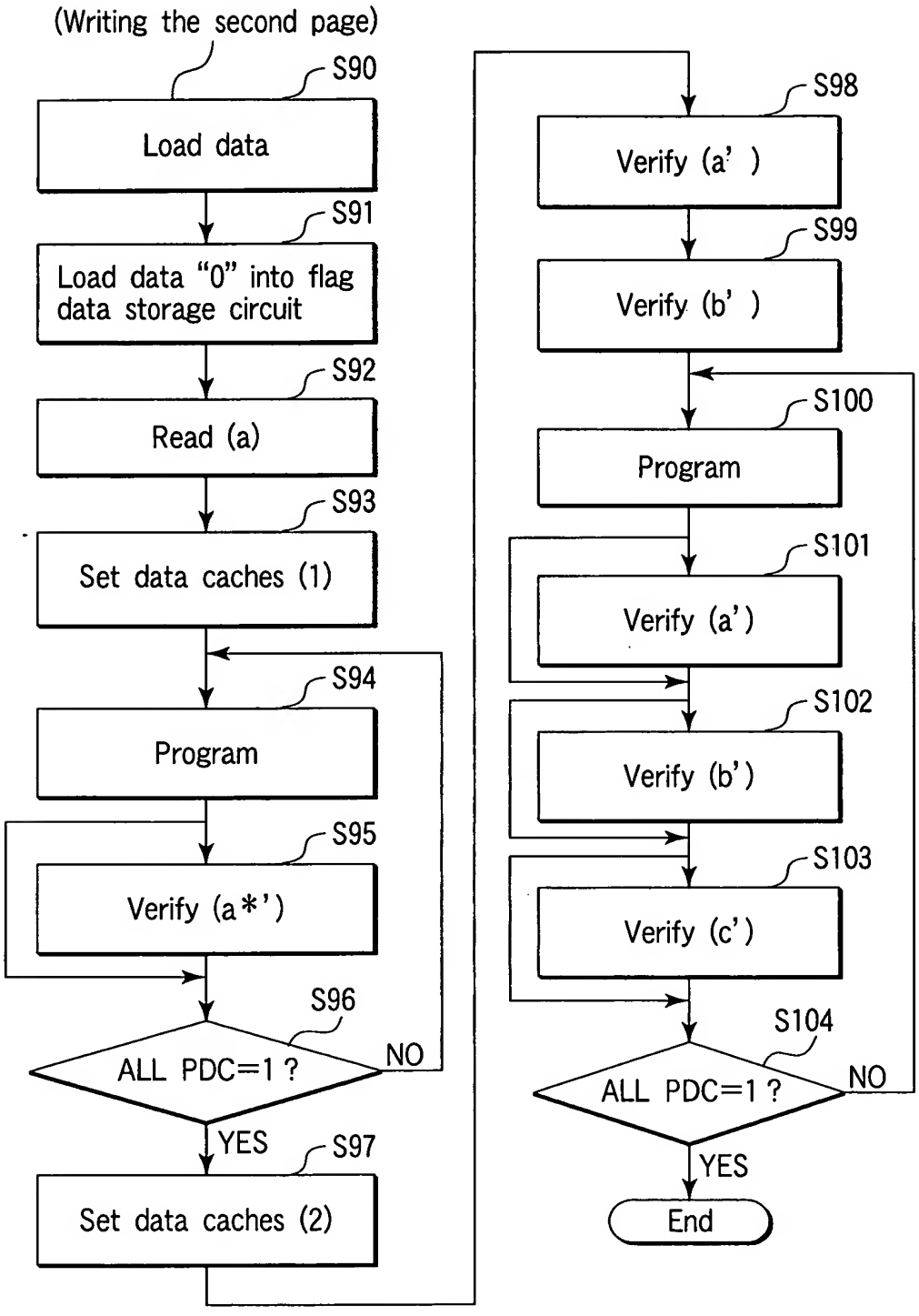
(Writing the second page)
S90
Load data
S91
Load data "0" into flag data storage circuit
S92
Read (a)
S93
Set data caches (1)
S94
Program
S95
Verify (a*')
S96
ALL PDC=1 ?
NO
YES
S97
Set data caches (2)
S98
Verify (a')
S99
Verify (b')
S100
Program
S101
Verify (a')
S102
Verify (b')
S103
Verify (c')
S104
ALL PDC=1 ?
NO
YES
End

FIG. 24

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	
DDC	0	0	1	1	
PDC	1	0	1	1	1 : Write unselected 0 : Write

FIG. 25

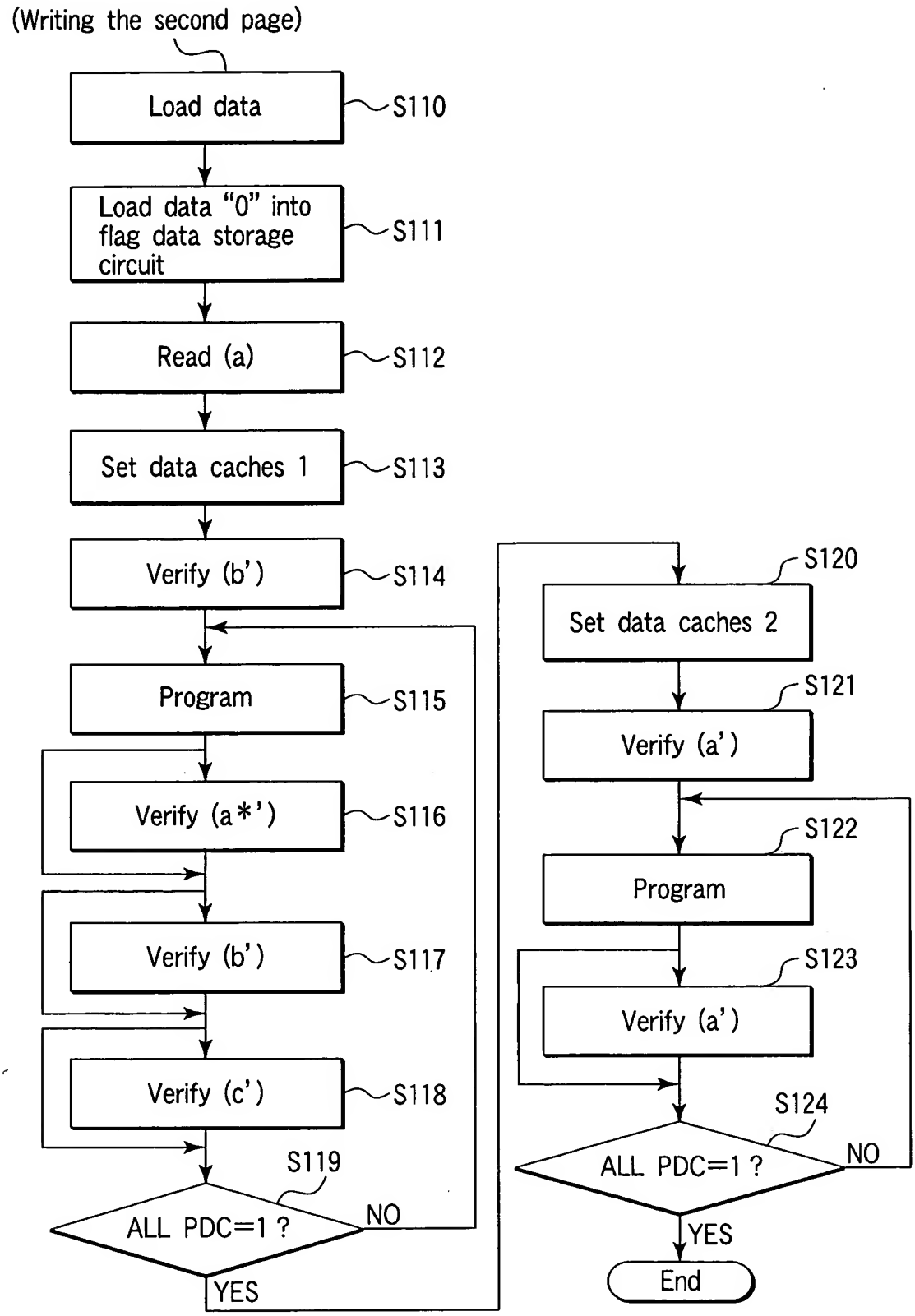
(Writing the second page)
Load data
S110
Load data "0" into flag data storage circuit
S111
Read (a)
S112
Set data caches 1
S113
Verify (b')
S114
Program
S115
Verify (a*')
S116
Verify (b')
S117
Verify (c')
S118
S119
ALL PDC=1 ?
NO
YES
S120
Set data caches 2
S121
Verify (a')
S122
Program
S123
Verify (a')
S124
ALL PDC=1 ?
NO
YES
End

FIG. 26

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	0	0	Used far charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 27A

Data cache setting 2

	Data in memory cell after writing				
	0	1	2	3	
PDC	1	0	1	1	1 : Write unselected 0 : Write

FIG. 27B

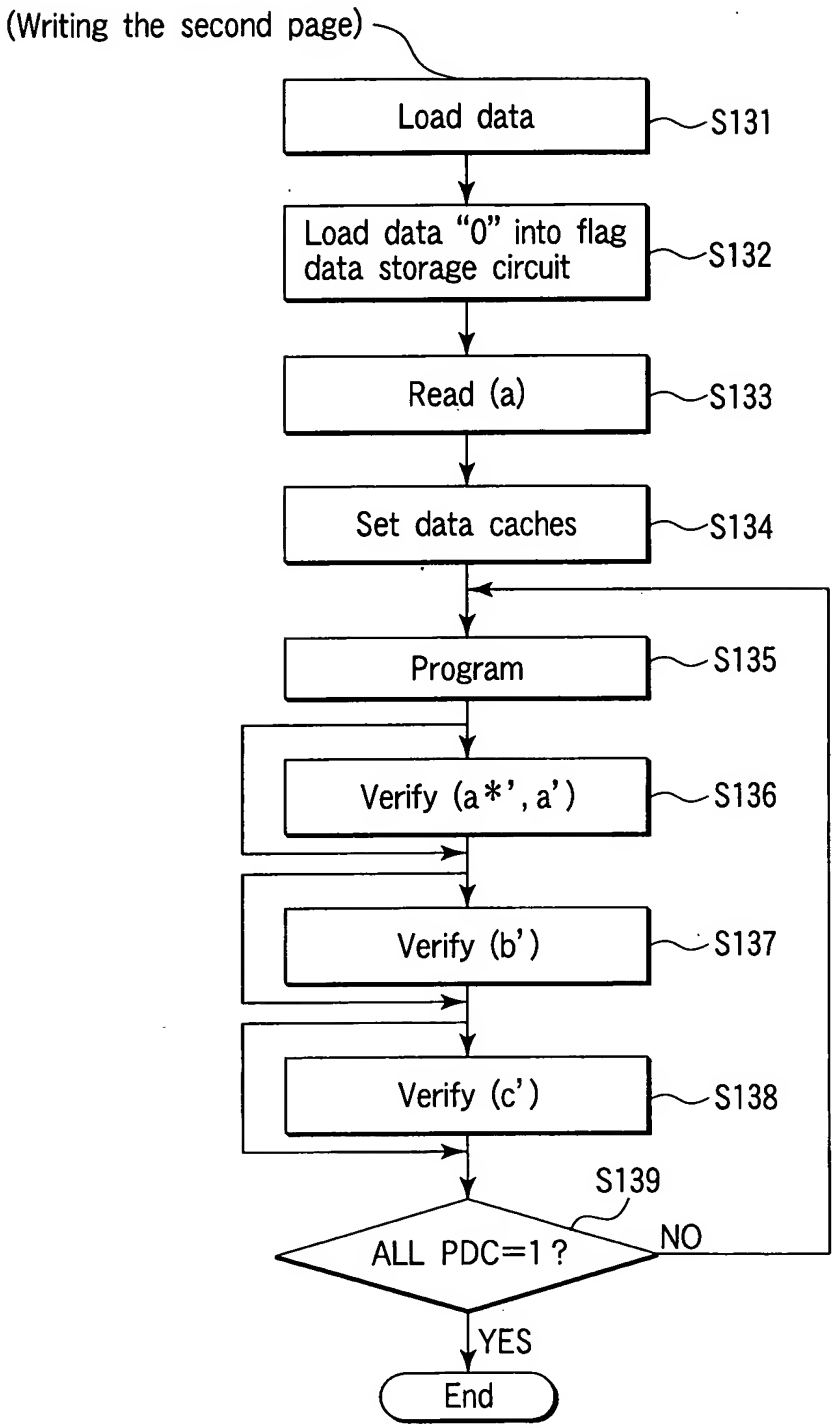
(Writing the second page)
Load data
S131
Load data "0" into flag data storage circuit
S132
Read (a)
S133
Set data caches
S134
Program
S135
Verify (a*', a')
S136
Verify (b')
S137
Verify (c')
S138
S139
ALL PDC=1 ?
NO
YES
End

FIG. 28

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 29A

After data cache setting

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1 : Write unselected 0 : Write

FIG. 29B

Precharge bit line on the basis of the data in DDC

	Data in memory cell after writing				
	0	1	2	3	
Bit line	Vdd	F (Vss)	Vdd	Vdd	

FIG. 30A

With BLC1 = Vclamp, connect PDC to bit line

	Data in memory cell after writing				
	0	1	2	3	
Bit line	Vdd	0/Inter-mediate	0	0	

FIG. 30B

During program recovery, transfer data in PDC to DCC, invent data in DDC, and transfer the inverted data to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	0	1	0	0	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 30C

Verify (a)
Charge bit line on the basis of data in PDC
Discharge bit line at a potential of WL = a*
Invert data in PDC while discharging bit line

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	1	0	1	1	Used far precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 31A

Load the potential of bit line into TDC
With VREG = H and REG = H, make TDC 1 when dynamic data is 1
Transfer data in PDC ta DDC and data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used far charging in verifying memory cell data 2
DDC	1	0	0	1	User for precharging bit line in programming and for chagrining in verifying memory cell data 1
PDC	1	0/1	1	1	1 : Write unselected 0 : Write

FIG. 31B

With WL = a', discharge bit line
With VREG = H and REG = H, set 1 in TDC when dynamic data is 1
Transfer data in PDC to DDC
Transfer data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 32A

Transfer data in DDC to PDC
Then, transfer data in PDC to DDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1 : Write unselected 0 : Write

FIG. 32B

With memory cell data 1, all of the writing with verify (a*) is completed
(the writing with verify (a') might nat be completed)

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used far charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

FIG. 33A

With memory cell data 1, all of the writing with verify (a') is completed
(the writing with verify (a') might not be completed)

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	1	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

FIG. 33B

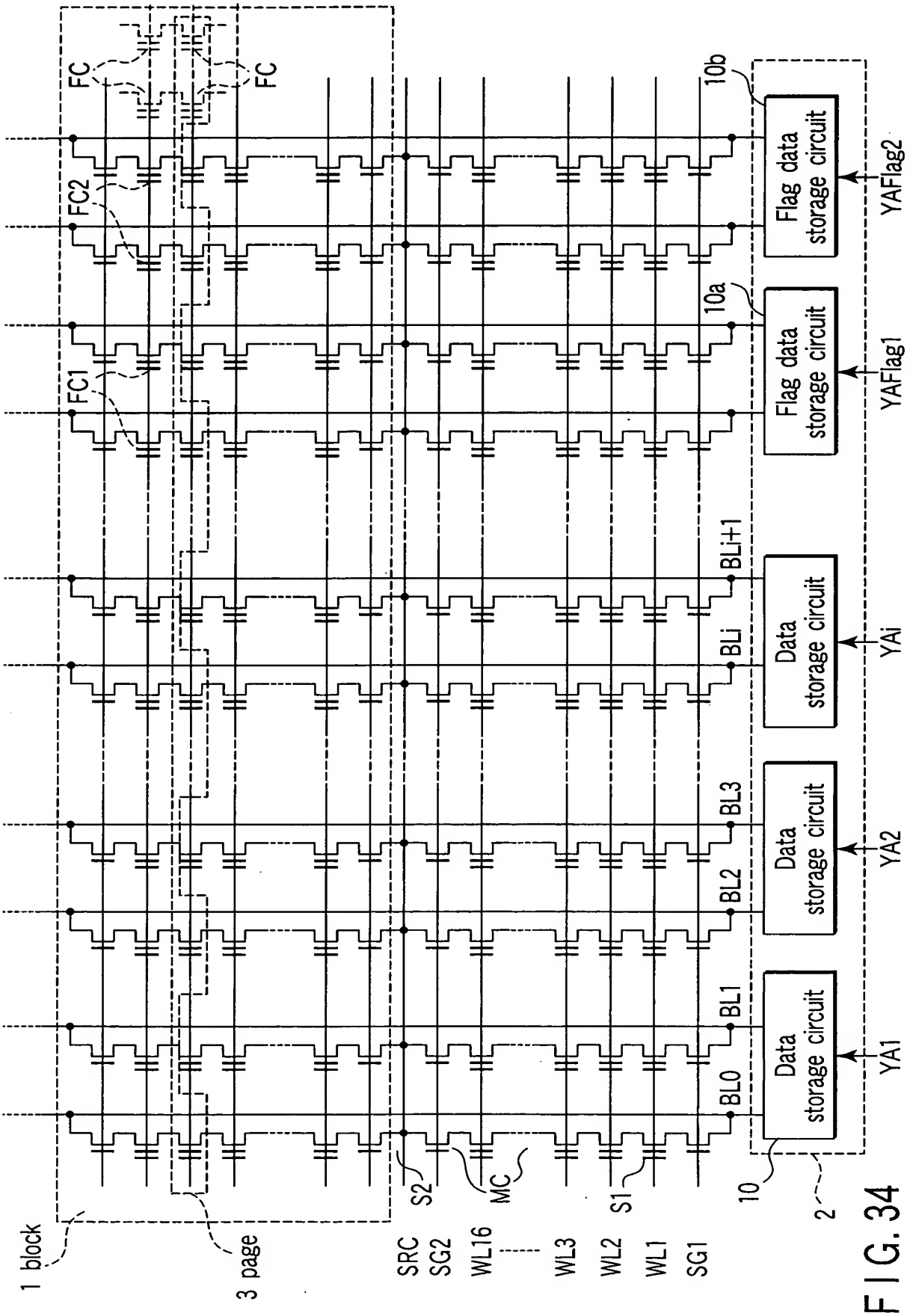
FC
FC
FC2
FC1
10b
10a
Flag data storage circuit
Flag data storage circuit
Data storage circuit
Data storage circuit
Data storage circuit
YAFlag2
YAFlag1
YAi
YA2
YA1
BLi+1
BLi
BL3
BL2
BL1
BL0
1 block
3 page
SRC
SG2
WL16
WL3
WL2
WL1
SG1
S2
MC
S1
10
2

FIG. 34

(After writing first page and before writing second page)

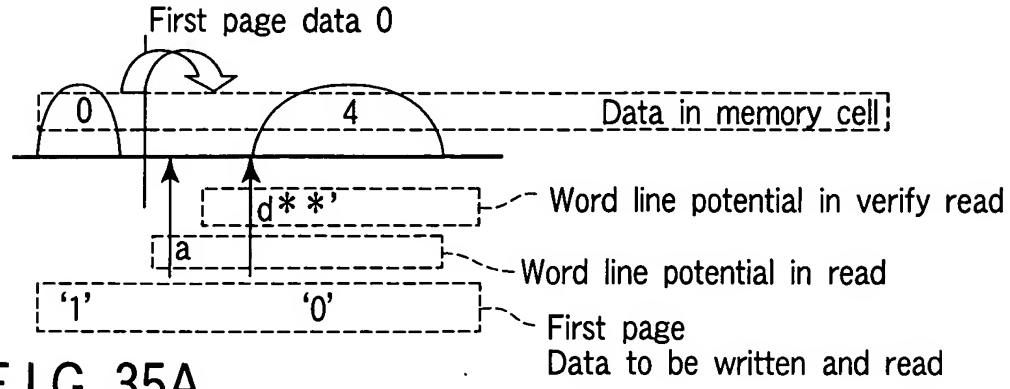

FIG. 35A

(After writing first page, before writing second page, and after writing adjacent cells of first page)

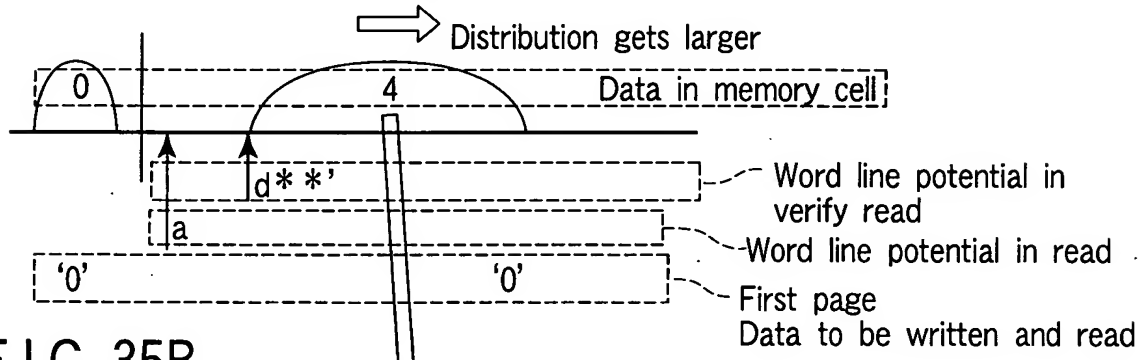

FIG. 35B

After writing second page, before writing third page, and after writing adjacent cells of second page

With first page data 1, second page data 0 is obtained

With first page data 0, second page data 1 is obtained

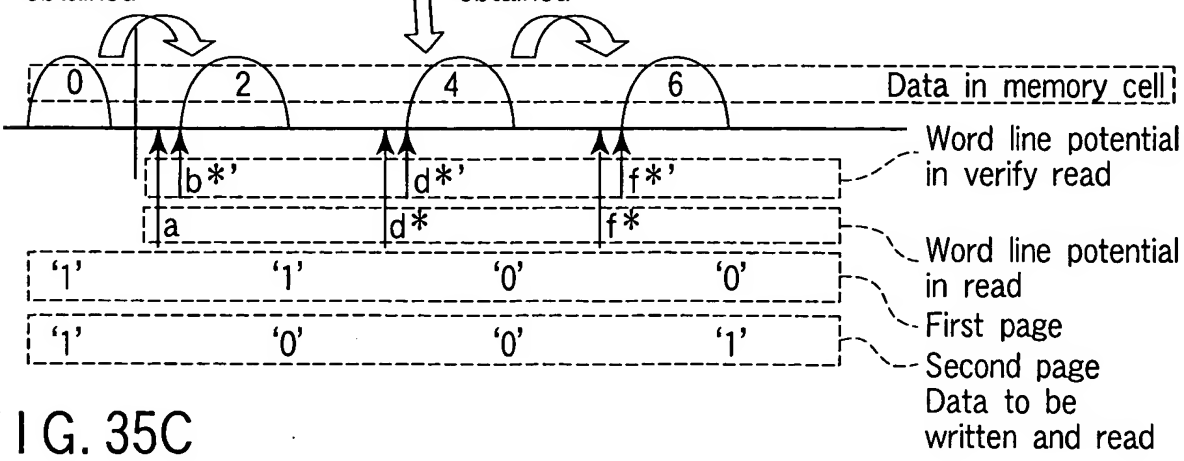

FIG. 35C

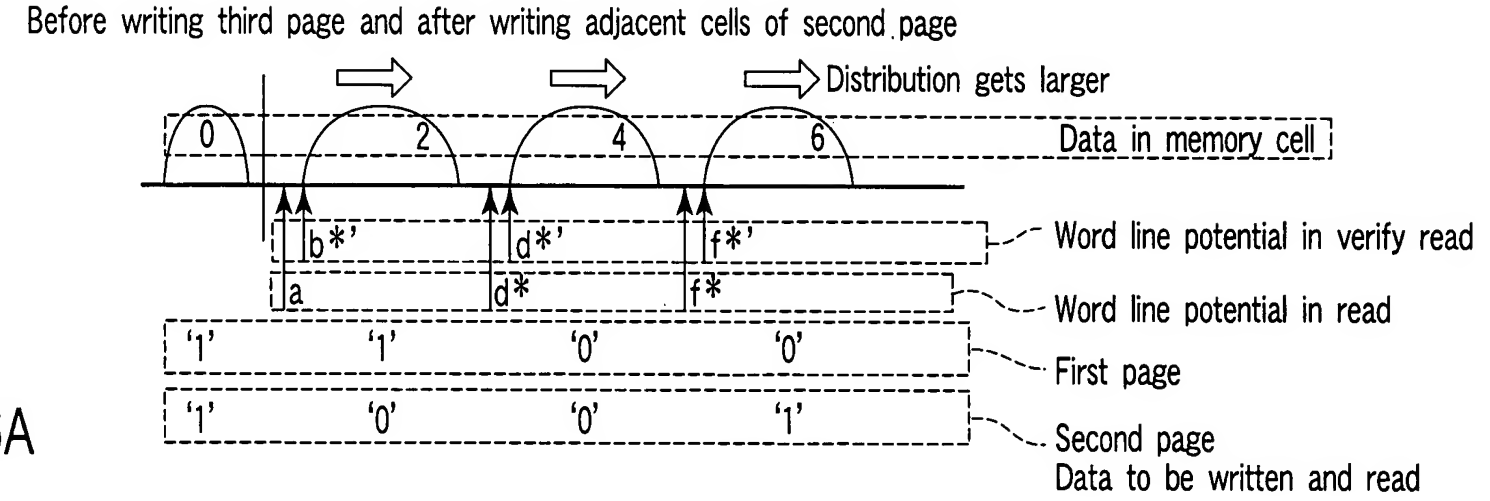

FIG. 36A

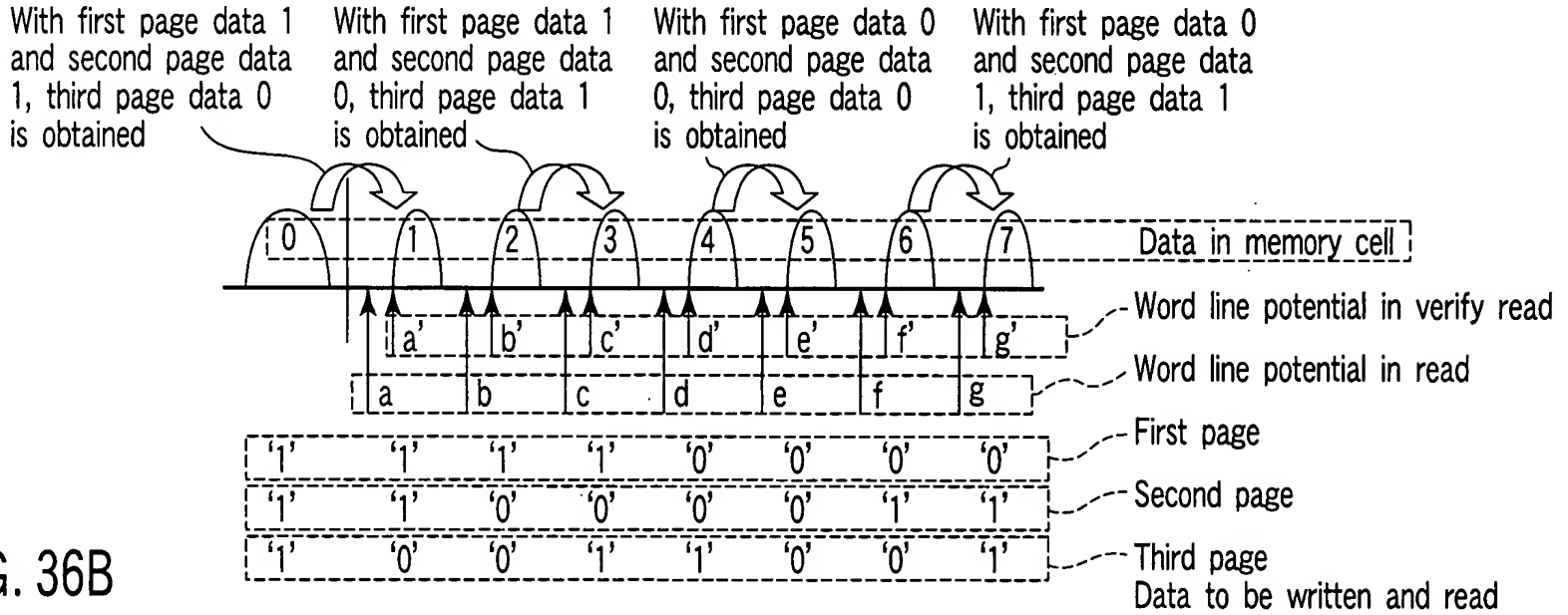

FIG. 36B

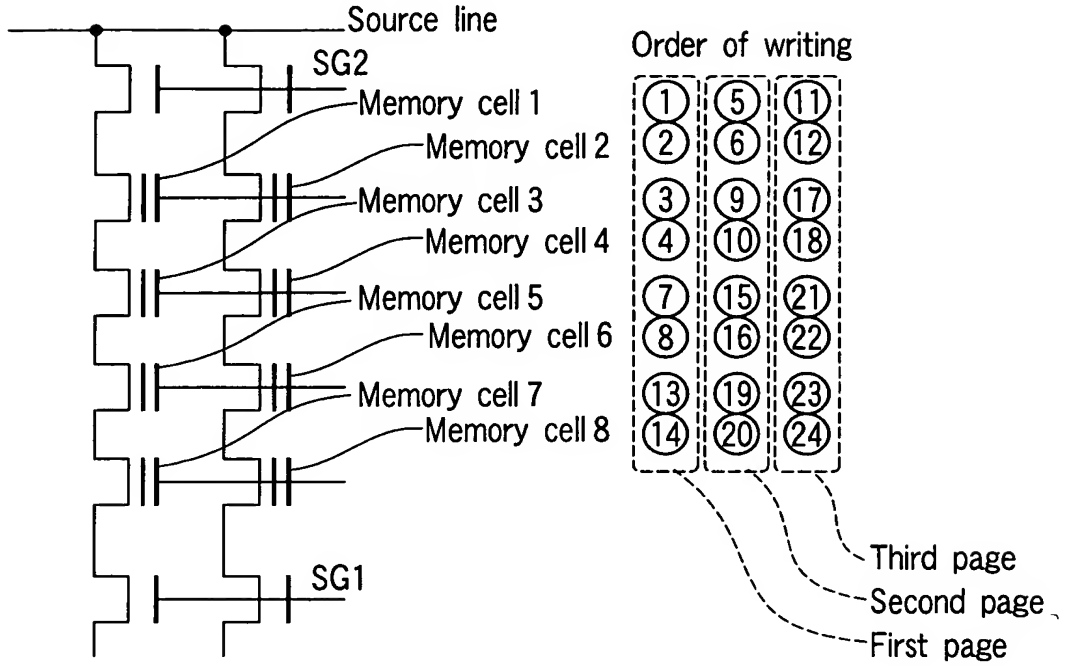

FIG. 37A

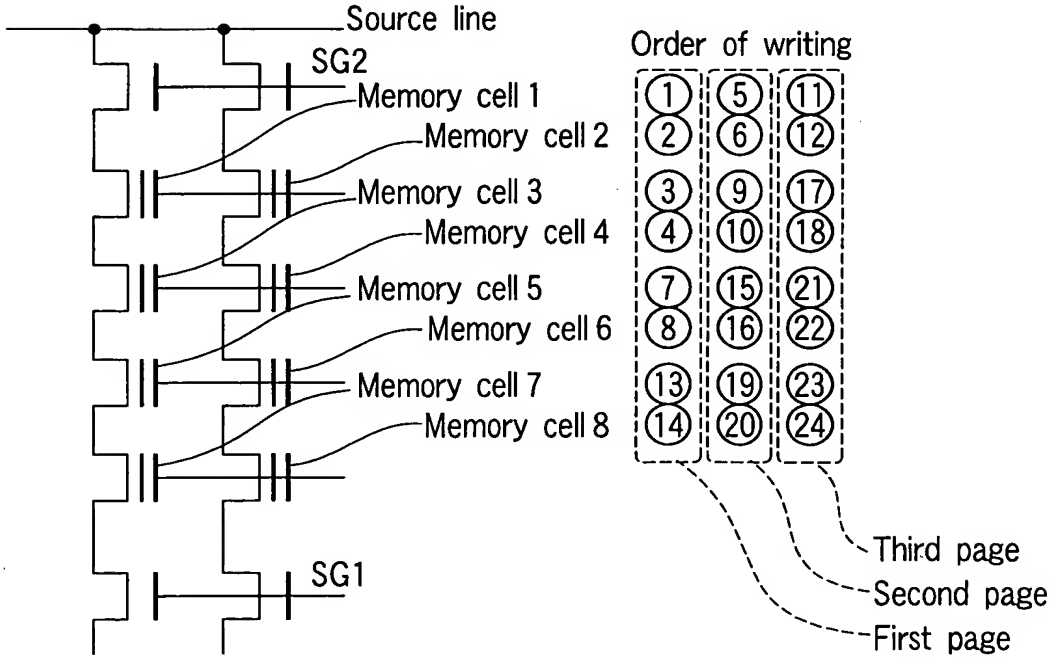

FIG. 37B

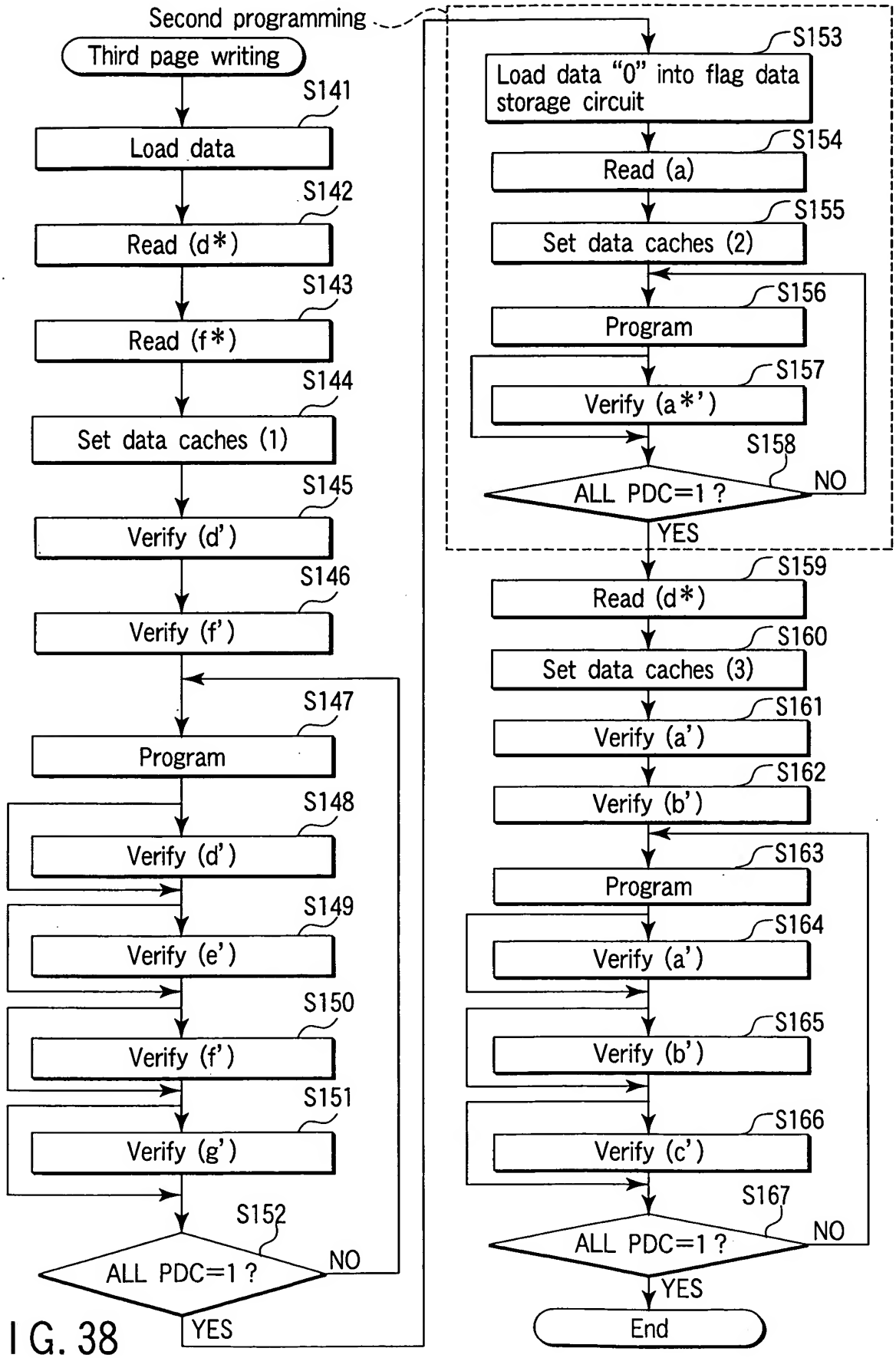
Second programming
Third page writing
S141
Load data
S142
Read (d*)
S143
Read (f*)
S144
Set data caches (1)
S145
Verify (d')
S146
Verify (f')
S147
Program
S148
Verify (d')
S149
Verify (e')
S150
Verify (f')
S151
Verify (g')
S152
ALL PDC=1 ?
NO
YES
S153
Load data "0" into flag data storage circuit
S154
Read (a)
S155
Set data caches (2)
S156
Program
S157
Verify (a*')
S158
ALL PDC=1 ?
NO
YES
S159
Read (d*)
S160
Set data caches (3)
S161
Verify (a')
S162
Verify (b')
S163
Program
S164
Verify (a')
S165
Verify (b')
S166
Verify (c')
S167
ALL PDC=1 ?
NO
YES
End

FIG. 38

After third page data load internal read 1

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	0	0	1	1	0	0	1	Data to be written and read inputted from the outside world
DDC	0	0	0	0	0	0	1	1	Data to be read by internal read
PDC	0	0	0	0	1	1	1	1	Data to be read by internal read

FIG. 39A

After third page data cache setting 1

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	1	1	1	1	1	0	0	Used far charging in verifying memory cell data items 5, 4
DDC	0	1	1	0	0	1	1	0	Used for charging in verifying memory cell data 6 Forced to be at VSS in verifying memory cell data 4
PDC	1	1	1	1	0	0	0	0	1 : Write unselected 0 : Write

FIG. 39B

After third page data cache setting 2

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	1	0	0	0	0	0	0	
DDC	0	1	1	0	0	1	1	0	
PDC	1	0	1	1	1	1	1	1	1 : Write unselected 0 : Write

FIG. 40A

After third page data cache setting 3

	Data in memory cell after writing								
	0	1	2	3	4	5	6	7	
SDC	1	1	0	0	0	0	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1	1	1	1	1 : Write unselected 0 : Write

FIG. 40B

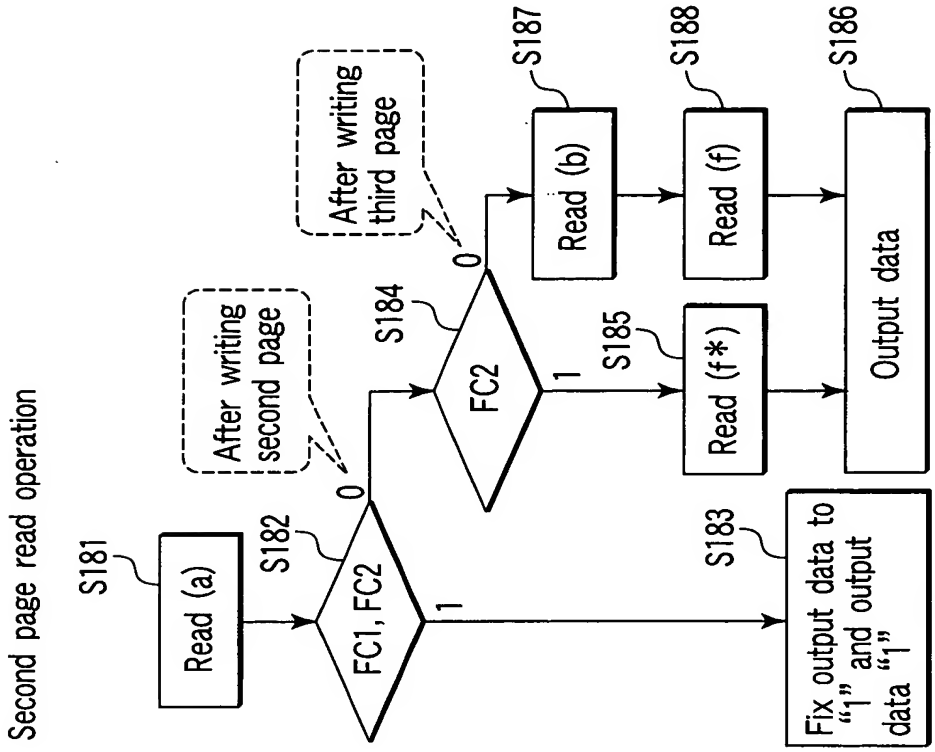

FIG. 41B

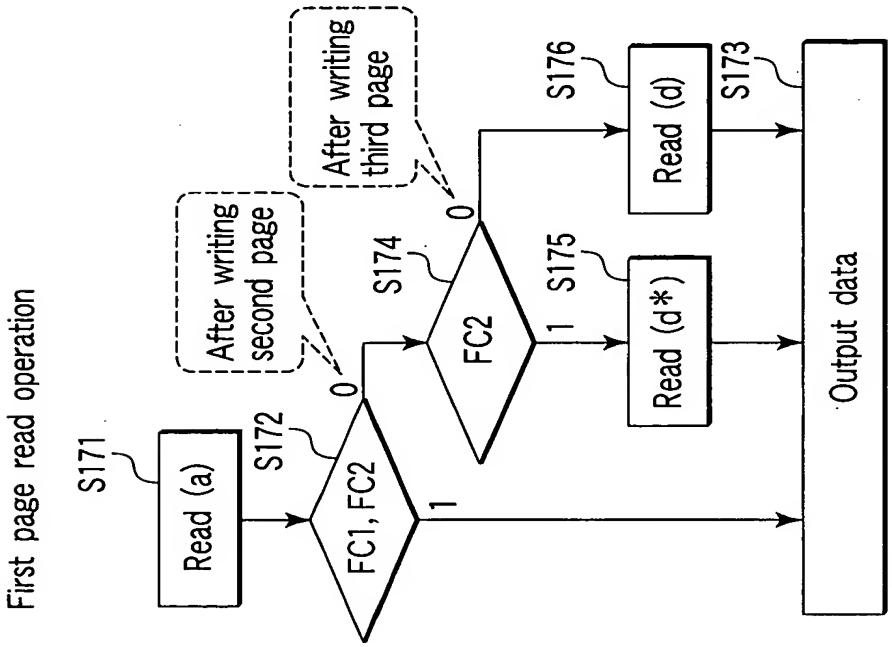

FIG. 41A

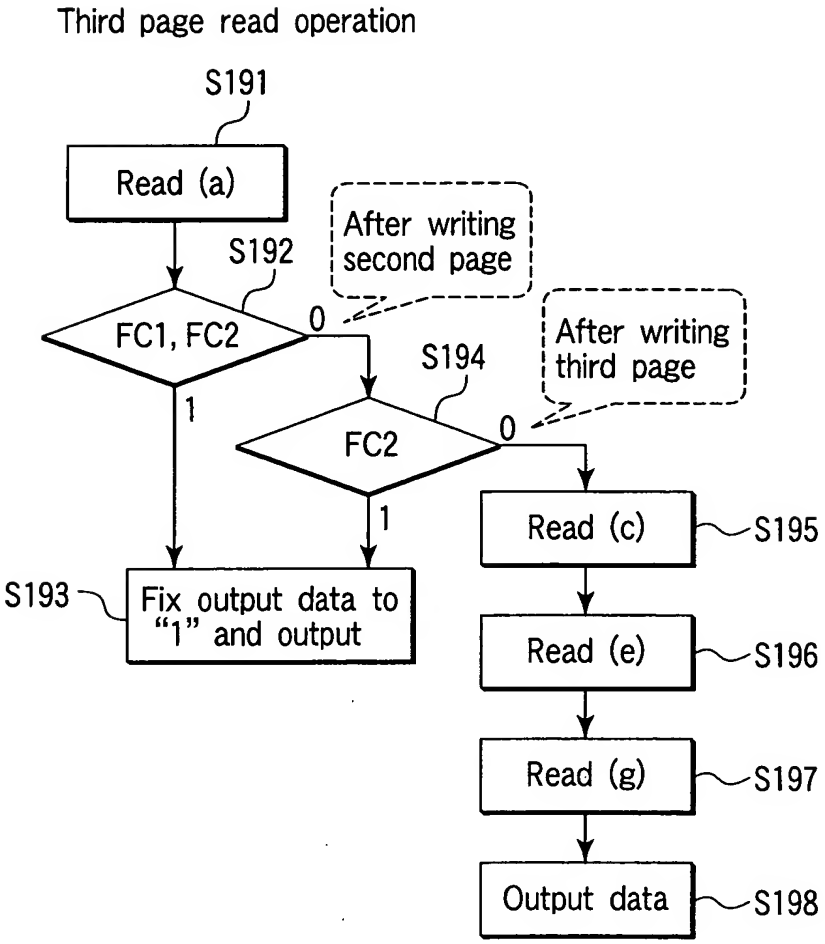
Third page read operation
S191
Read (a)
S192
FC1, FC2
0
1
After writing second page
S194
FC2
0
1
After writing third page
S193
Fix output data to "1" and output
Read (c)
S195
Read (e)
S196
Read (g)
S197
Output data
S198

FIG. 42

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 43A

After setting data caches

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	0	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected, 0 : Write

FIG. 43B

Verify (a*')
Charge bit line on the basis of data in SDC
Discharge bit line at a potential of WL=a*'

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	0	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected, 0 : Write

FIG. 44A

Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H
With VREG=H, REG=H, make TDC 1 when dynamic data is 1
Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	1	0	0	0	1 : Write unselected, 0 : Write
PDC	0	0/1	1	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a*' → 1

FIG. 44B

Discharge bit line at a potential of WL=a'
Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H
With VREG=H, REG=H, make TDC 1 when dynamic data is 1
Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing					
	0	1pass	1fail	2	3	
SDC	1	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	0/1	1	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a*' → 1
PDC	1	1	0	0	0	1 : Write unselected, 0 : Write

FIG. 45A

Verify (b')
Charge bit line on the basis of data in DDC
Discharge bit line at a potential of WL=b'
Transfer data in DDC to TDC, PDC to DDC and TDC to PDC during the discharge
Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H
With VREG=H, REG=H, make TDC 1 when dynamic data is 1
Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing					
	0	1	2fail	2pass	3	
SDC	1	1	0	0	0	Used for charging in verifying memory cell data 1
DDC	0	0/1	1	1	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a*' → 1
PDC	1	0	0	1	0	1 : Write unselected, 0 : Write

FIG. 45B

Verify (c)
Charge bit line
Discharge bit line at a potential of WL=c'
Transfer data in DDC to TDC, PDC to DDC and TDC to PDC during the discharge
Set Vdd in TDC and transfer the potential of bit line to TDC when BLCLAMP is H
With VREG=H, REG=H, make TDC 1 when dynamic data is 1
Transfer data in PDC to DDC and data in TDC to DDC

	Data in memory cell after writing					
	0	1	2	3fail	3pass	
SDC	1	1	0	0	0	Used for charging in verifying memory cell data 1
DDC	0	0/1	1	0	0	Used for charging in verifying memory cell data 2 When threshold voltage in memory cell into which data 1 is written exceeds a*' → 1
PDC	1	0	0	0	1	1 : Write unselected, 0 : Write

FIG. 46

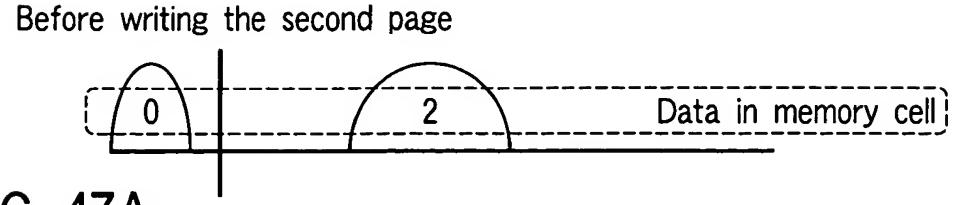

FIG. 47A

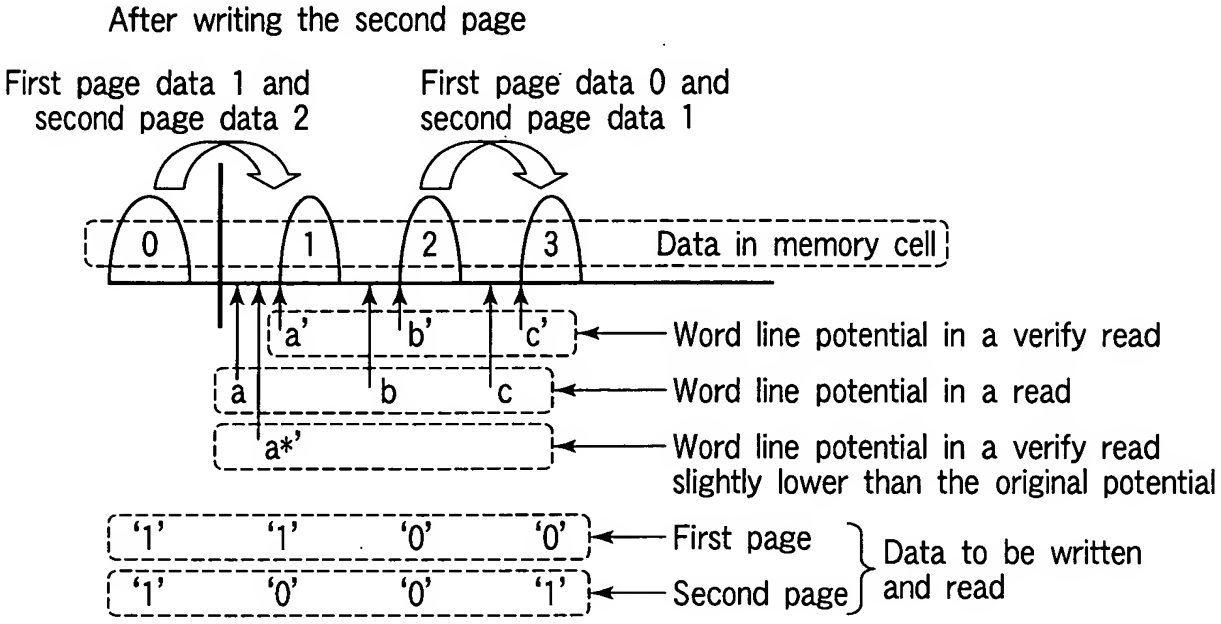

FIG. 47B

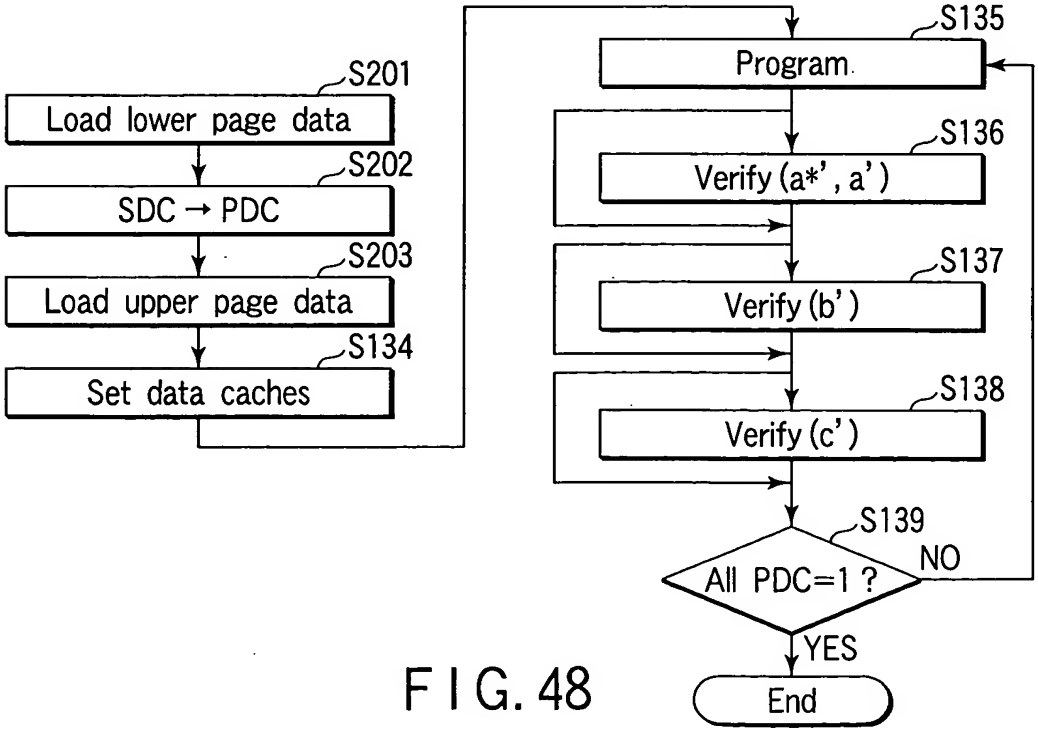

FIG. 48

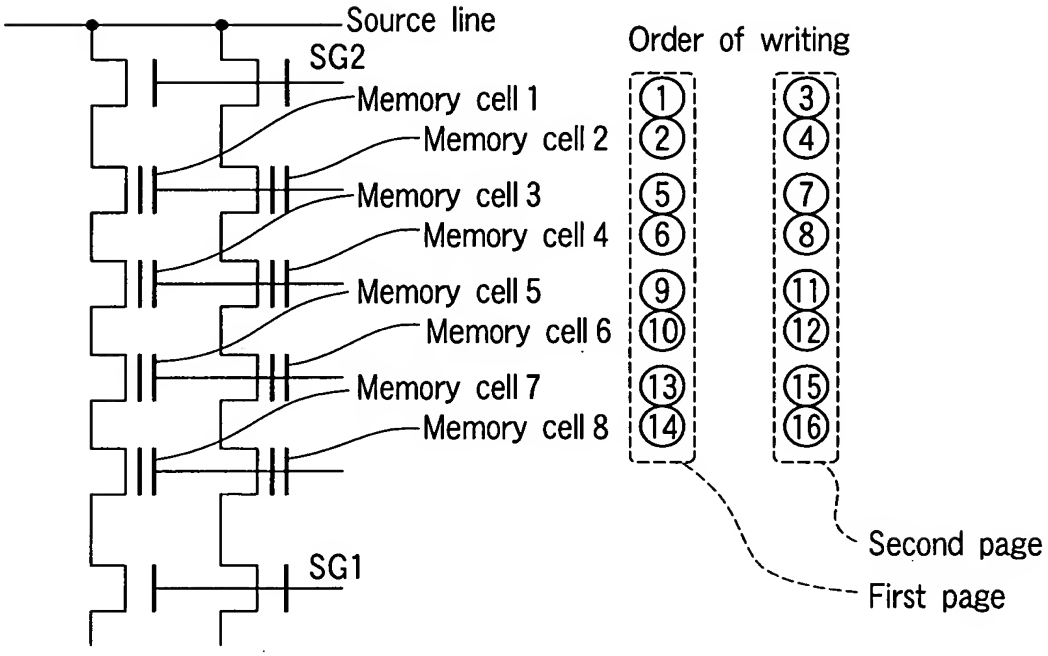
Source line
SG2
Memory cell 1
Memory cell 2
Memory cell 3
Memory cell 4
Memory cell 5
Memory cell 6
Memory cell 7
Memory cell 8
SG1
Order of writing
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
Second page
First page

FIG. 49

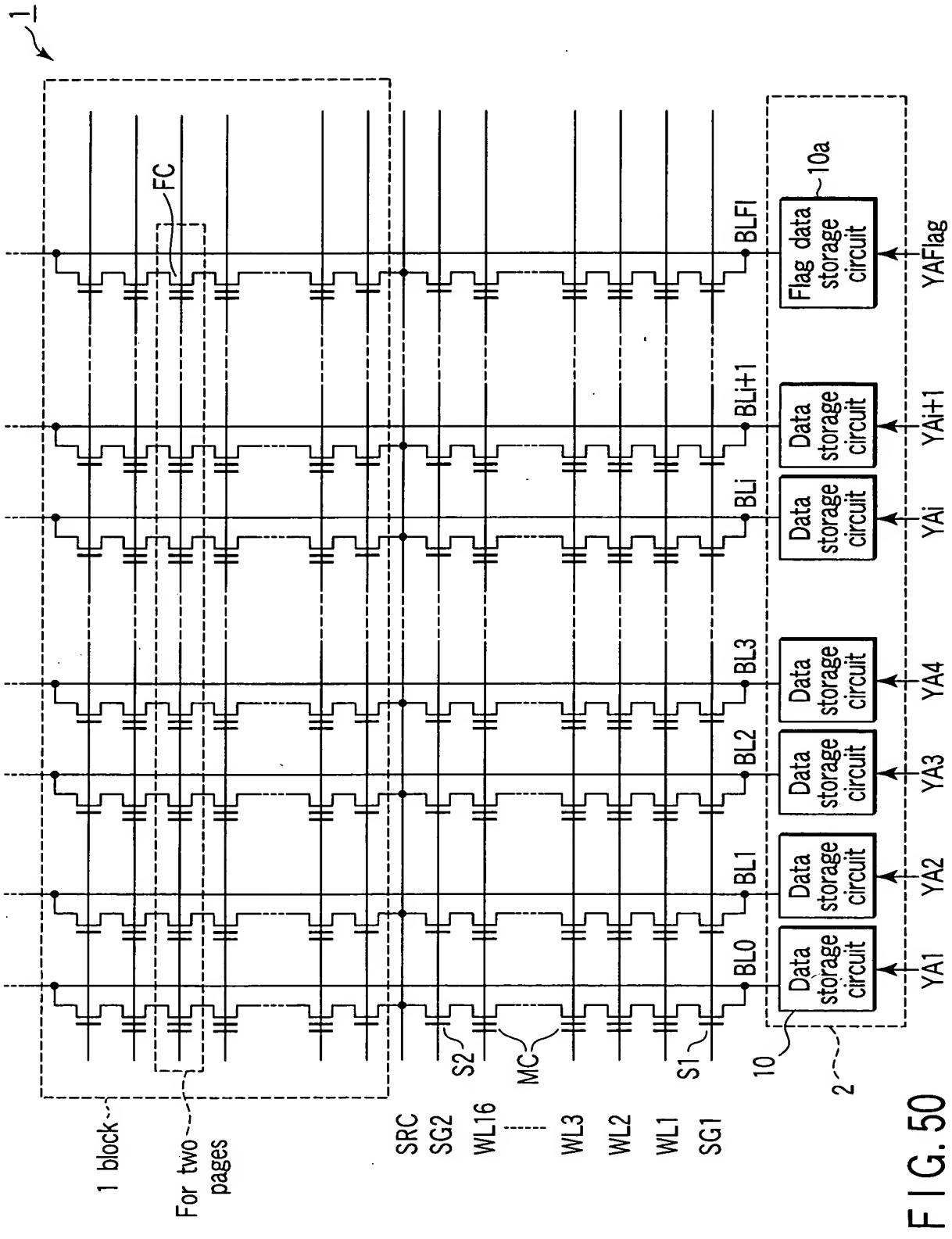
1
FC
BLFl
BLi+1
BLi
BL3
BL2
BL1
BL0
Flag data storage circuit
10a
Data storage circuit
YAFlag
YAi+1
YAi
YA4
YA3
YA2
YA1
10
2
S2
MC
S1
SRC
SG2
WL16
WL3
WL2
WL1
SG1
1 block
For two pages

FIG. 50

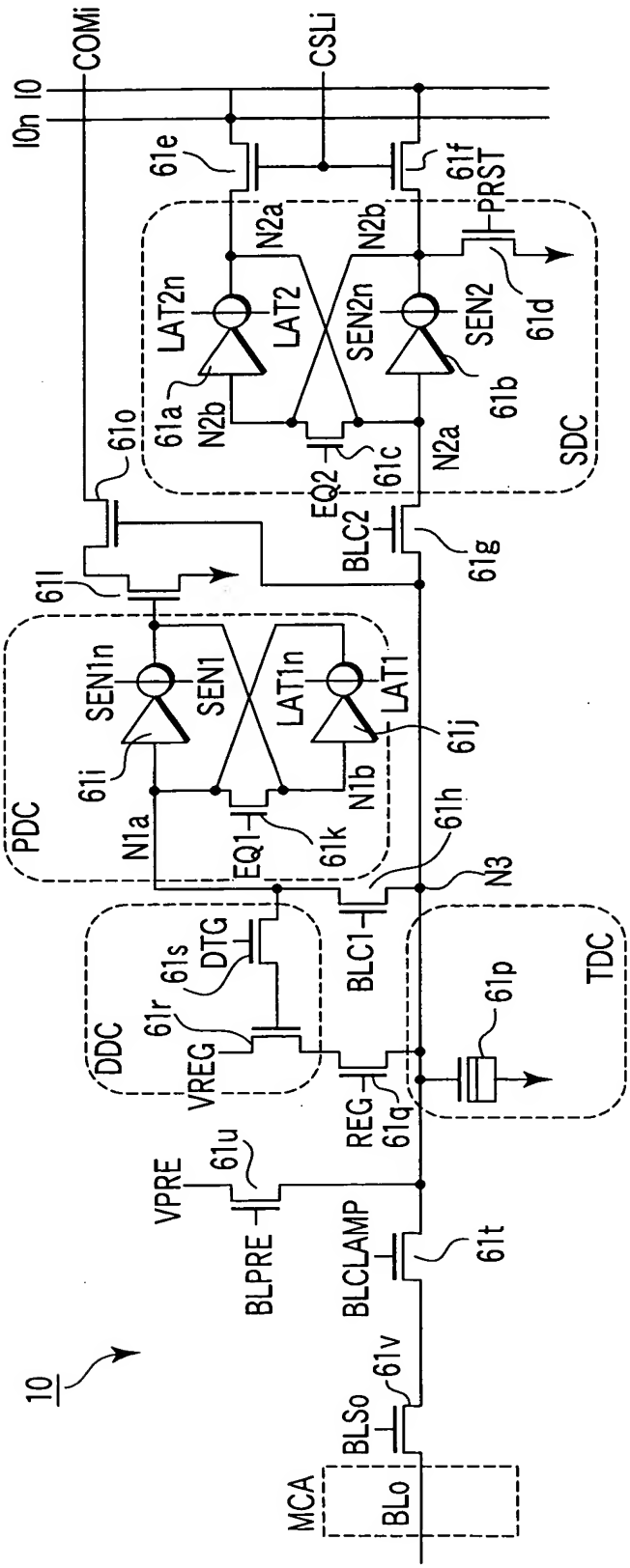
IOn IO
COMi
CSLi
61e
61f
PRST
N2a
N2b
LAT2n
LAT2
SEN2n
SEN2
61d
61a
61b
61o
61c
EQ2
BLC2
61g
SDC
61l
SEN1n
SEN1
LAT1n
LAT1
61i
61j
N1a
N1b
EQ1
61k
61h
N3
PDC
BLC1
DTG
61s
61r
VREG
DDC
TDC
61p
REG
61q
VPRE
61u
BLPRE
BLCLAMP
61t
61v
BLSo
MCA
BLo
10

FIG. 51

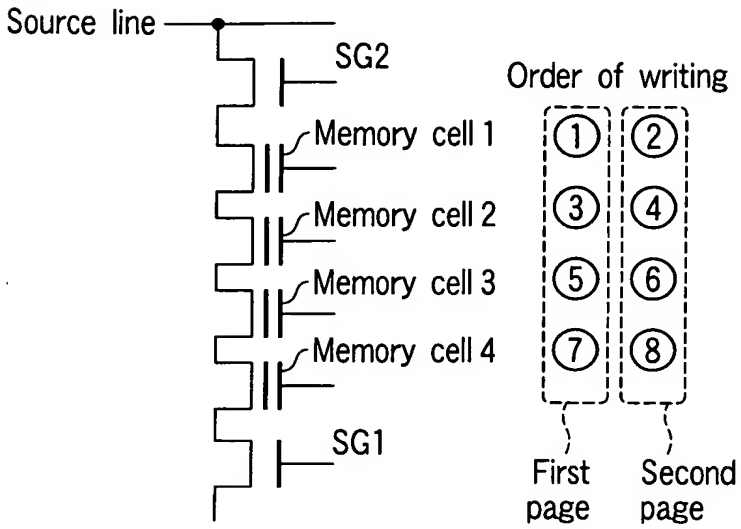
Source line
SG2
Memory cell 1
Memory cell 2
Memory cell 3
Memory cell 4
SG1
Order of writing
1
2
3
4
5
6
7
8
First page
Second page

FIG. 52

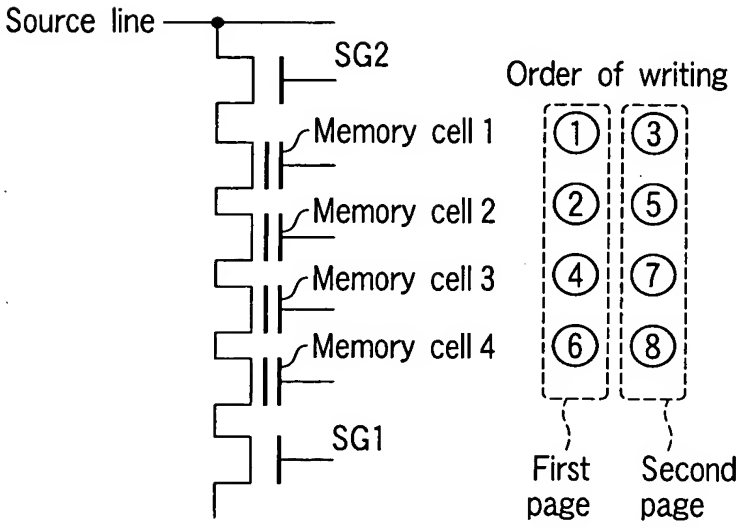
Source line
SG2
Memory cell 1
Memory cell 2
Memory cell 3
Memory cell 4
SG1
Order of writing
1
3
2
5
4
7
6
8
First page
Second page

FIG. 53

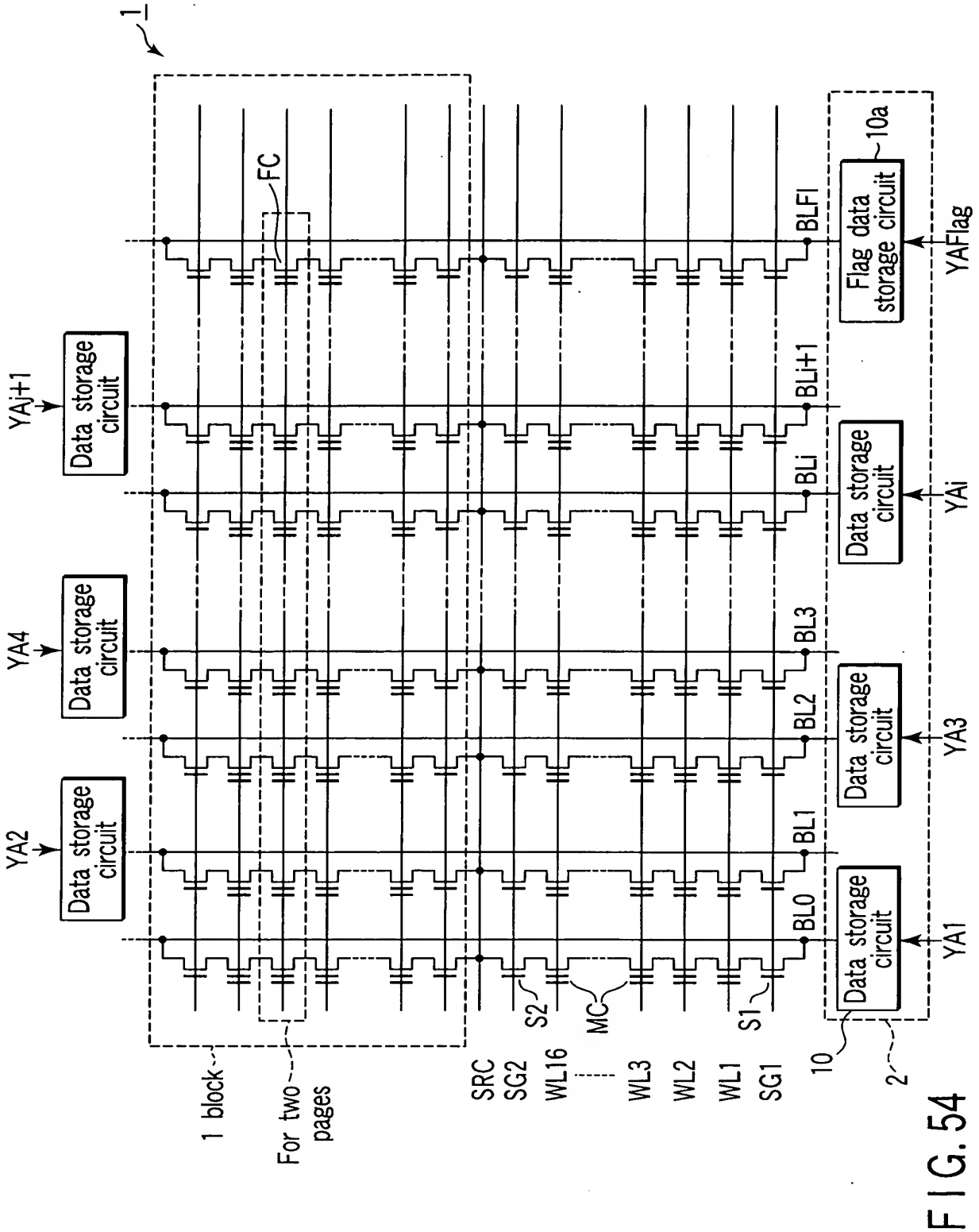
1
FC
BLFl
BLi+1
BLi
BL3
BL2
BL1
BL0
Flag data storage circuit
10a
YAFlag
YAj+1
YA4
YA2
YAi
YA3
YA1
Data storage circuit
1 block
For two pages
SRC
SG2
WL16
WL3
WL2
WL1
SG1
S2
MC
S1
10
2

FIG. 54

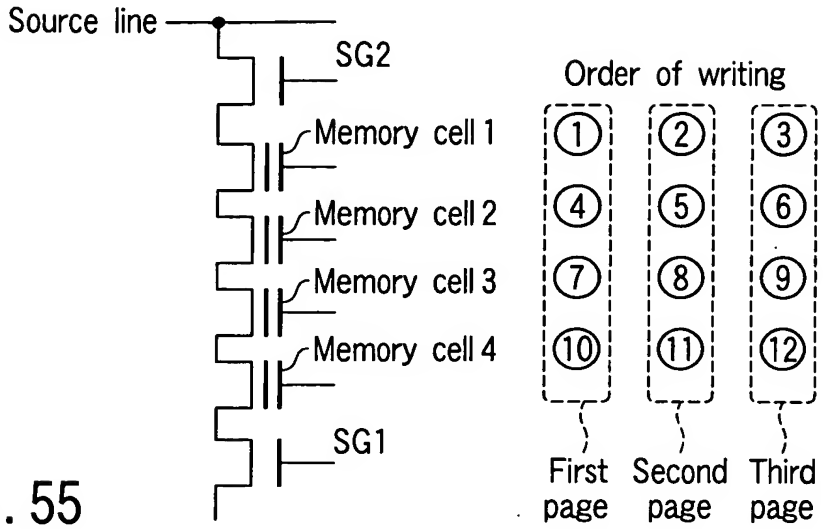

FIG. 55

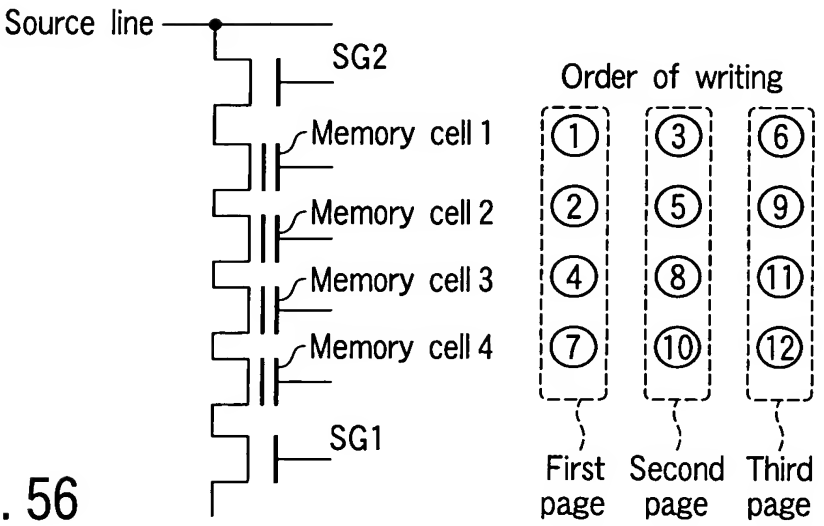

FIG. 56

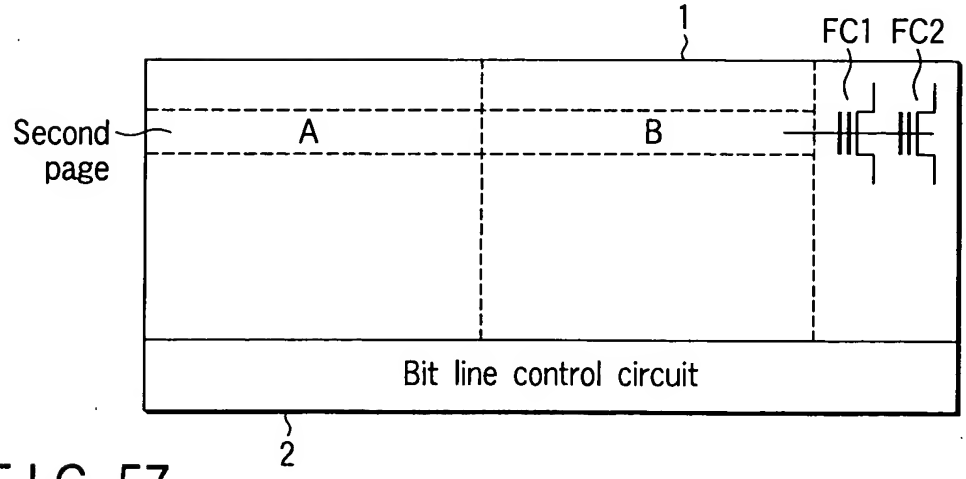

FIG. 57

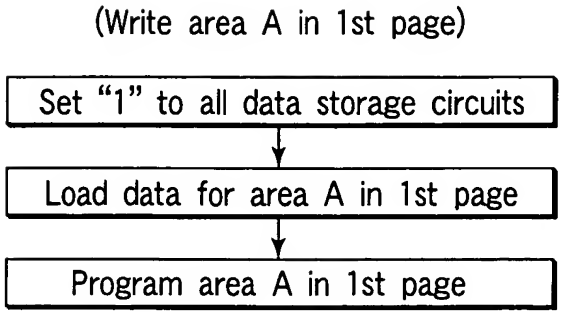

FIG. 58A

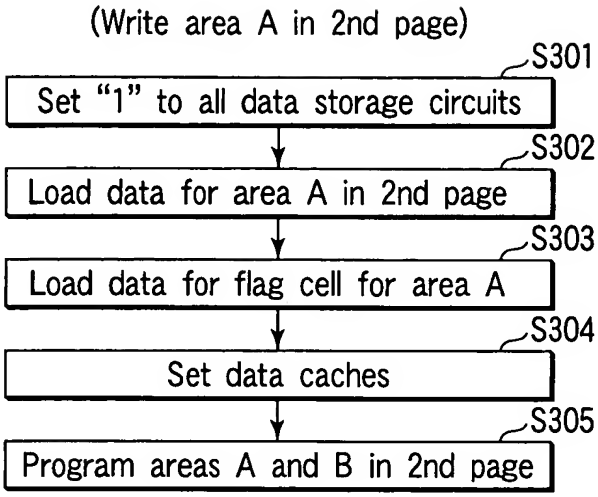

FIG. 58C

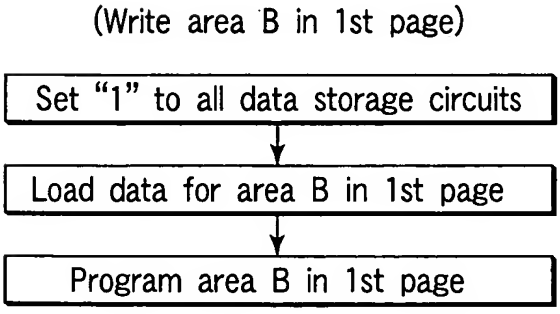

FIG. 58B

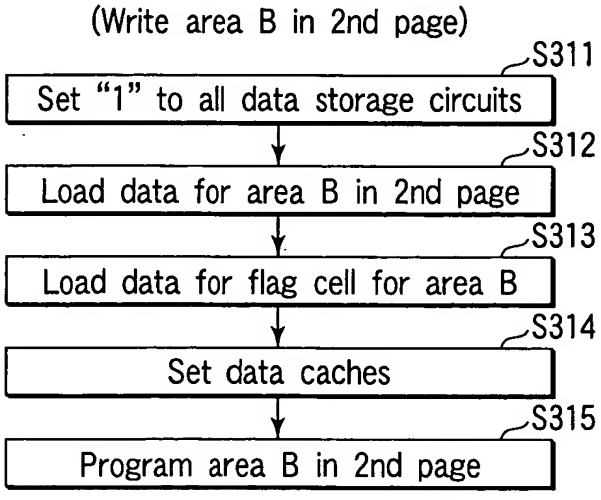

FIG. 58D

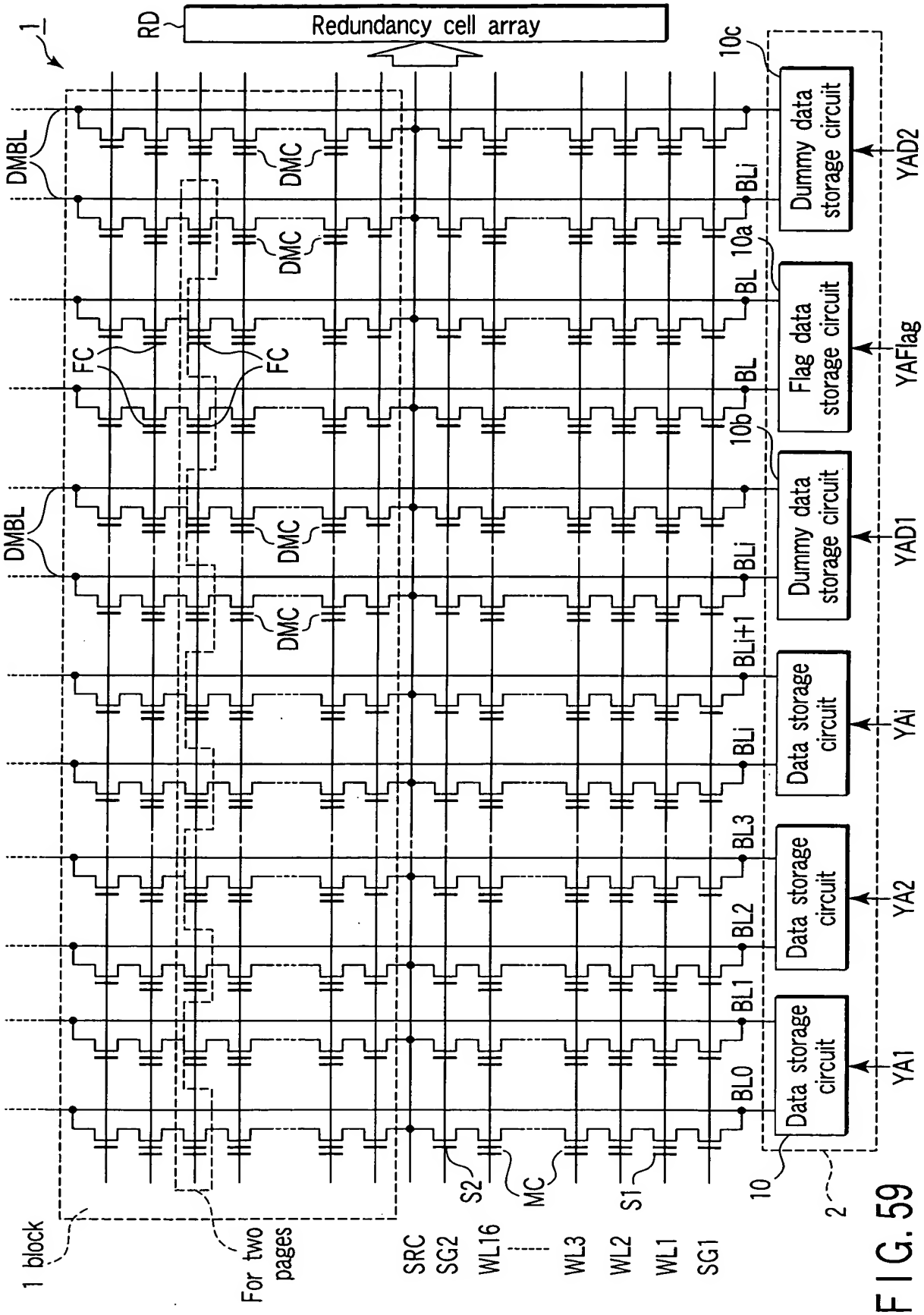
1
RD
Redundancy cell array
10c
Dummy data storage circuit
YAD2
BLi
10a
BL
Flag data storage circuit
YAFlag
10b
Dummy data storage circuit
YAD1
BLi+1
BLi
Data storage circuit
YAi
BL3
BL2
BL1
BL0
Data storage circuit
YA2
Data storage circuit
YA1
10
2
DMBL
DMC
FC
S2
MC
S1
1 block
For two pages
SRC
SG2
WL16
WL3
WL2
WL1
SG1

FIG. 59

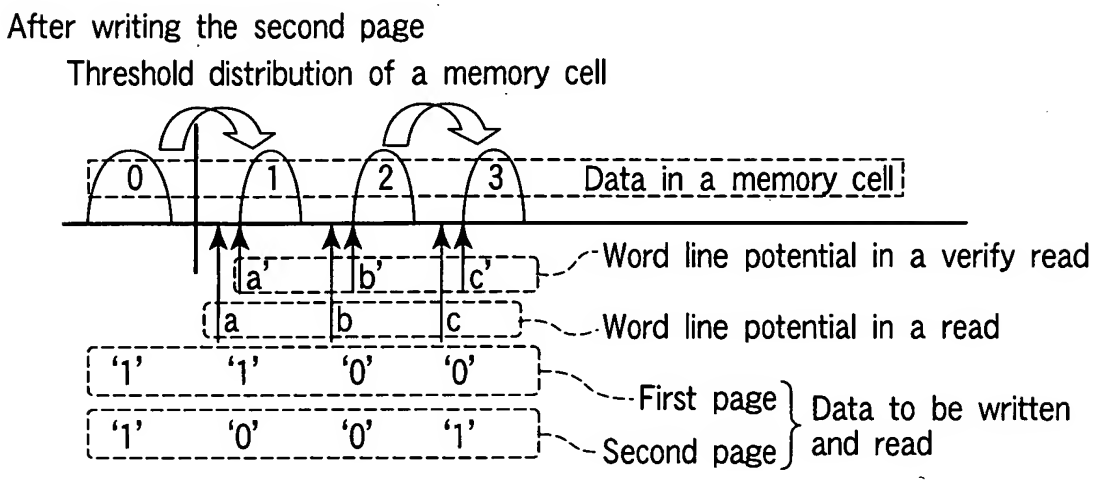

FIG. 60A

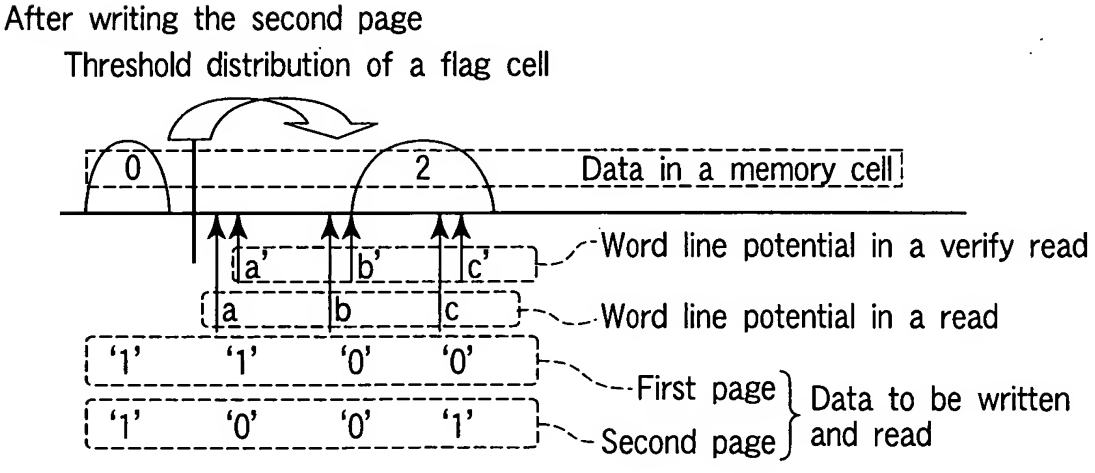

FIG. 60B

After writing the second page

Threshold distribution of the first flag cell

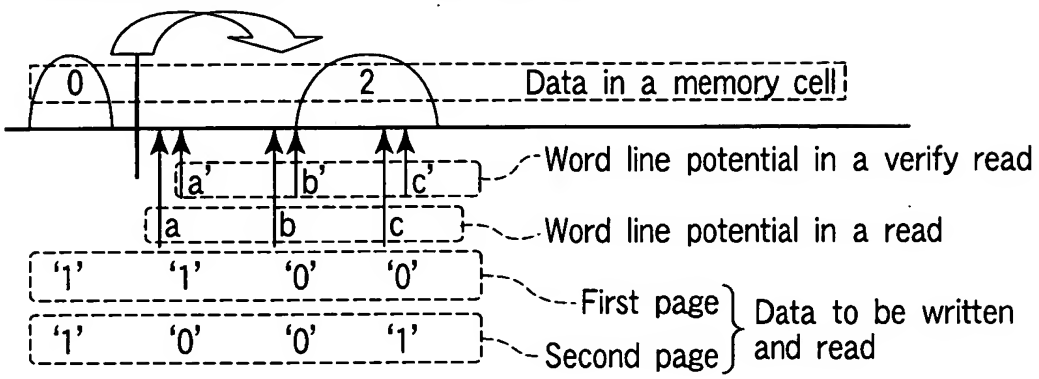

FIG. 61A

After writing the second page

Threshold distribution of the second flag cell

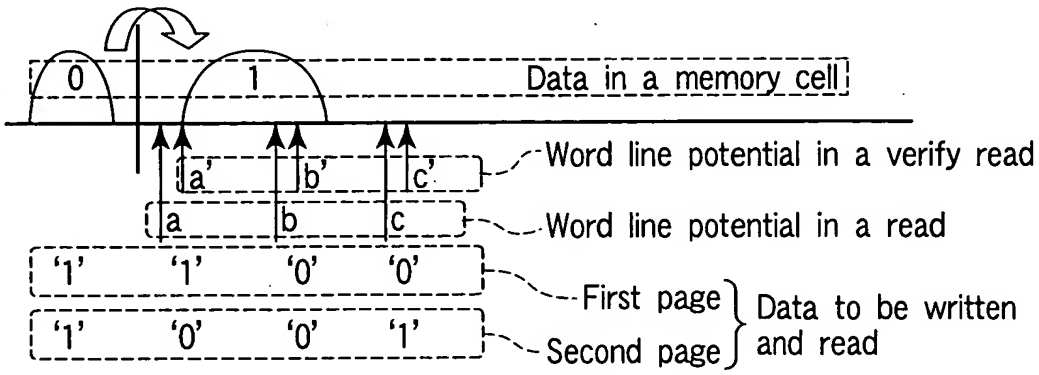

FIG. 61B

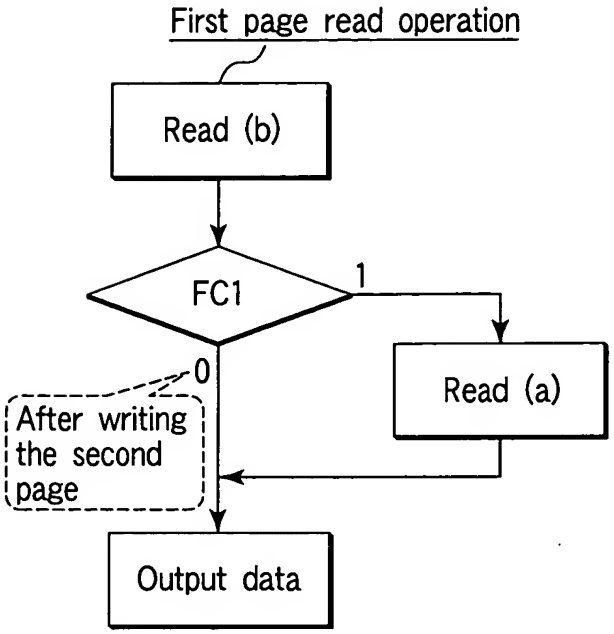

FIG. 62

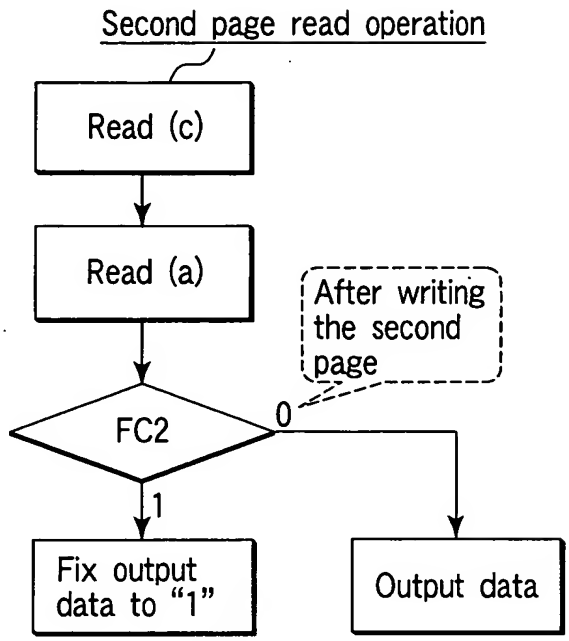

FIG. 63

Memory cell array	BL E	BL 0	BL 0	BL E	BL 0	BL E	BL 0	BL E	BL 0	BL 0	BL E	BL 0	BL E	BL 0	BL E	BL 0
	Dummy cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Dummy cell	Dummy cell	First flag cell	Second flag cell	First flag cell	Second flag cell	First flag cell	Second flag cell	Dummy cell

FIG. 64